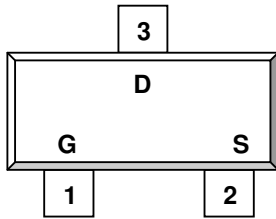


**PIN CONFIGURATION**  
**SOT-23**

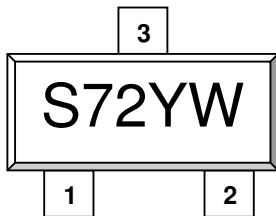


1.Gate 2.Source 3.Drain

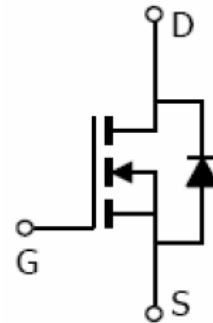
**FEATURE**

- 60V/0.30A,  $R_{DS(ON)} = 5\Omega$  @  $V_{GS} = 10V$ (Typ.)
- 60V/0.25A,  $R_{DS(ON)} = 7\Omega$ @  $V_{GS} = 4.5V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and Maximum DC current capability
- SOT-23 package design

**PART MARKING**  
**SOT-23**



Y : Year Code W : Process Code





**2N7002** 

N Channel Enhancement Mode MOSFET

300mA

**ABSOLUTE MAXIMUM RATINGS** (Ta = 25°C Unless otherwise noted )

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V <sub>DSS</sub>	60	V
Gate-Source Voltage	V <sub>GSS</sub>	±20	V
Continuous Drain Current (T <sub>J</sub> =150°C)	I <sub>D</sub>	0.3	A
	T <sub>A</sub> =25°C		
Pulsed Drain Current	I <sub>DM</sub>	1.0	A
Power Dissipation	P <sub>D</sub>	0.35	W
	T <sub>A</sub> =25°C		
Operation Junction Temperature	T <sub>J</sub>	150	°C
Storage Temperature Range	T <sub>STG</sub>	-55/150	°C
Thermal Resistance-Junction to Ambient	R <sub>θJA</sub>	375	°C/W



**2N7002** 

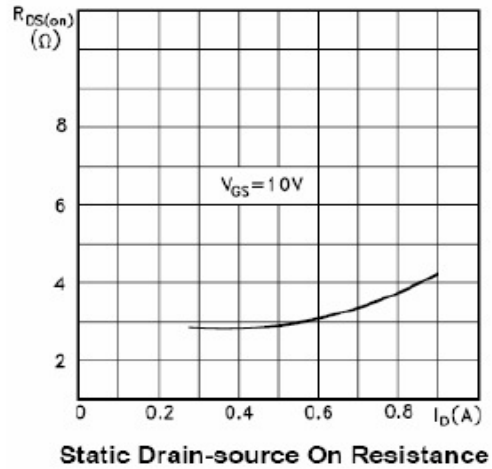
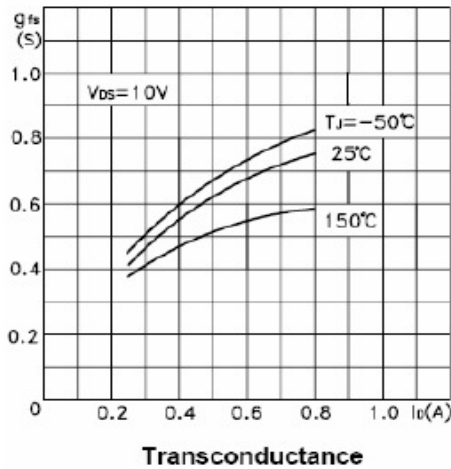
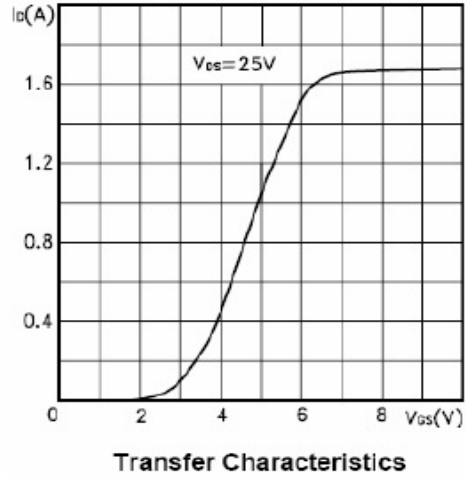
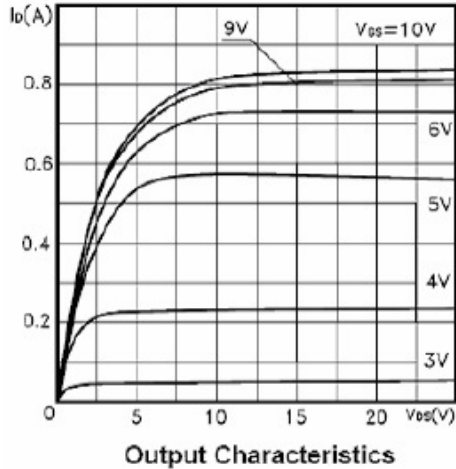
N Channel Enhancement Mode MOSFET

**300mA**

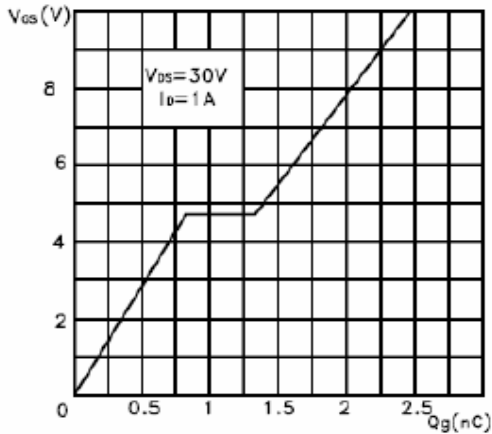
**ELECTRICAL CHARACTERISTICS** ( Ta = 25°C Unless otherwise noted )

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D= 250\mu A$	60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D= 250\mu A$	0.8		2.5	V
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 12V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}= 45V, V_{GS}=0V$			1	uA
		$V_{DS}= 45V, V_{GS}=0V$ $T_J=125^\circ C$			10	
On-State Drain Current	$I_{SD(on)}$				0.35	A
On-State Drain Current (pulsed)	$I_{SDM(2)}$				1.4	
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=10.0V, I_D=0.50A$		2.50	6.0	$\Omega$
		$V_{GS}=4.5V, I_D= 0.25A$		3.30	7.0	
Forward Transconductance	$G_{fs(1)}$	$V_{DS}=10V, I_D= 0.5A$		0.6		S
Diode Forward Voltage	$V_{SD(1)}$	$I_S=0.12A, V_{GS}=0V$		0.85	1.5	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=30V, V_{GS}=4.5V$ $I_D= 1.0A$		1.4	2.0	nC
Gate-Source Charge	$Q_{gs}$			0.8		
Gate-Drain Charge	$Q_{gd}$			0.5		
Input Capacitance	$C_{iss}$	$V_{DS}=25V, f=1MHz,$ $V_{GS}=0$		43		pF
Output Capacitance	$C_{oss}$			20		
Reverse Transfer Capacitance	$C_{rss}$			6		
Turn-On Time	$t_{d(on)tr}$	$V_{DD}=30V$ $I_D=0.5A$ $V_{GS}=4.5V$ $R_G=4.7\Omega$		6		nS
				15		
Turn-Off Time	$t_{d(off)tf}$			6	13	
				7	9	

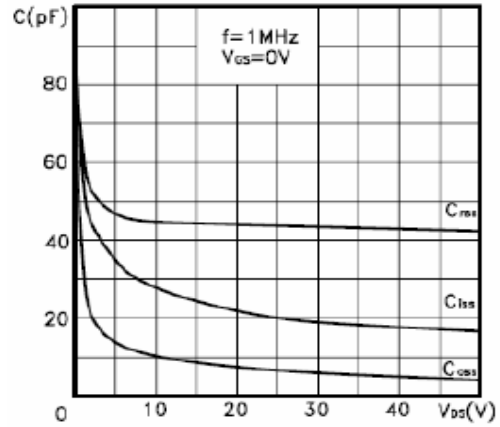
**TYPICAL CHARACTERISTICS** (25°C Unless noted)



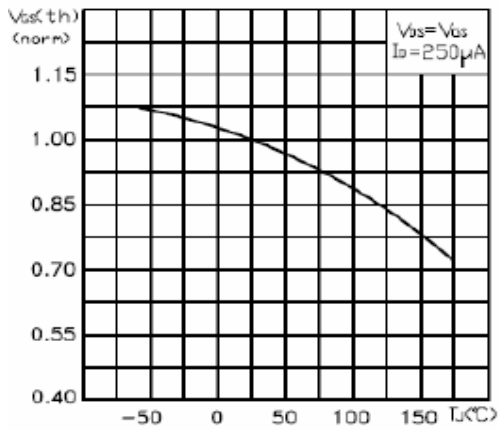
**TYPICAL CHARACTERISTICS**



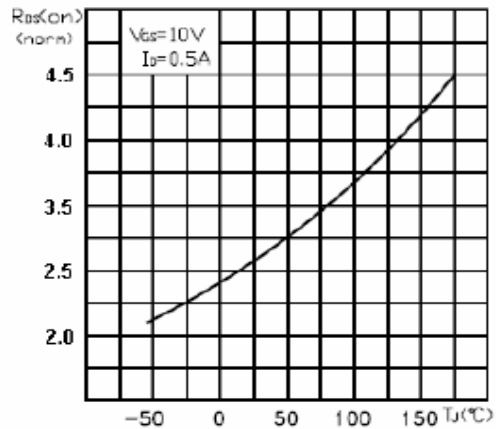
**Gate Charge vs Gate-source Voltage**



**Capacitance Variations**

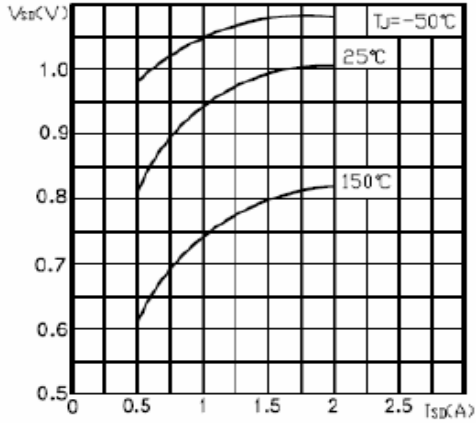


**Normalized Gate Threshold Voltage vs Temperature**

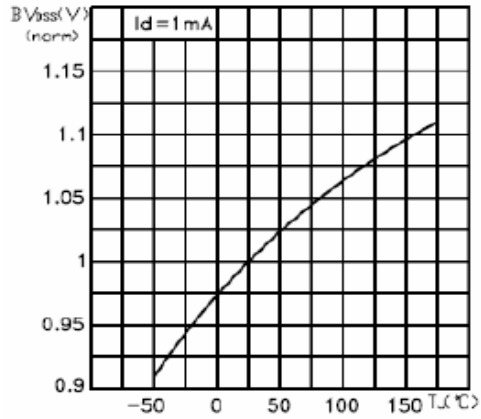


**Normalized On Resistance vs Temperature**

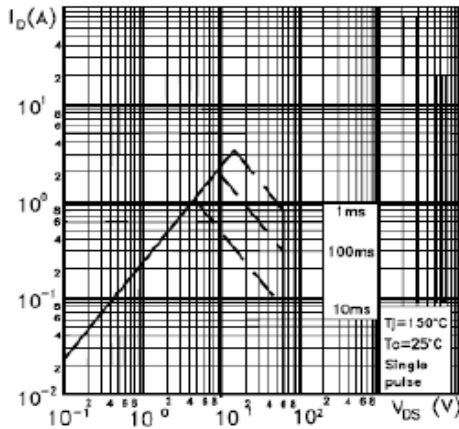
**TYPICAL CHARACTERISTICS**



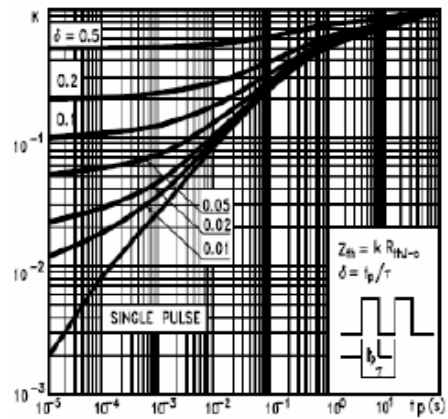
**Source-Drain Forward**



**Normalized BVDSS vs Temperature**

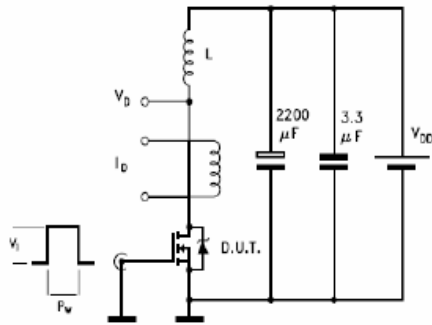


**Safe Operating Area**

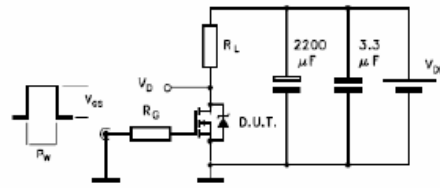


**Thermal Impedance**

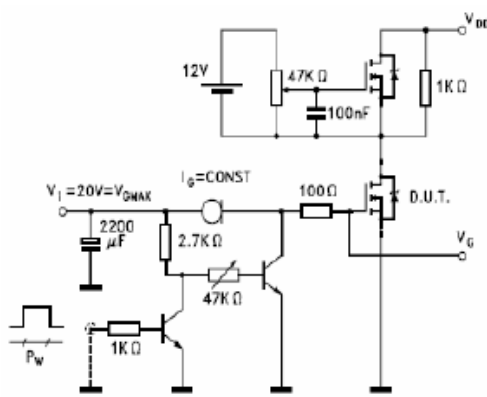
**TIPYCAL TESTING CIRCUIT**



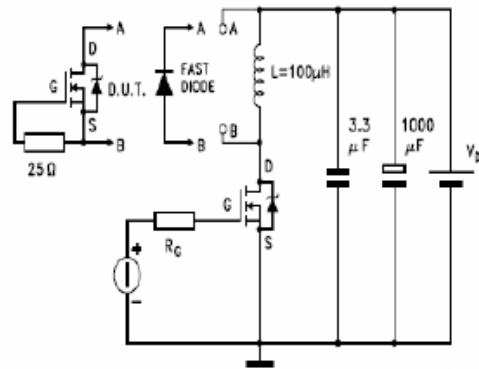
**Unclamped Inductive Load Test**



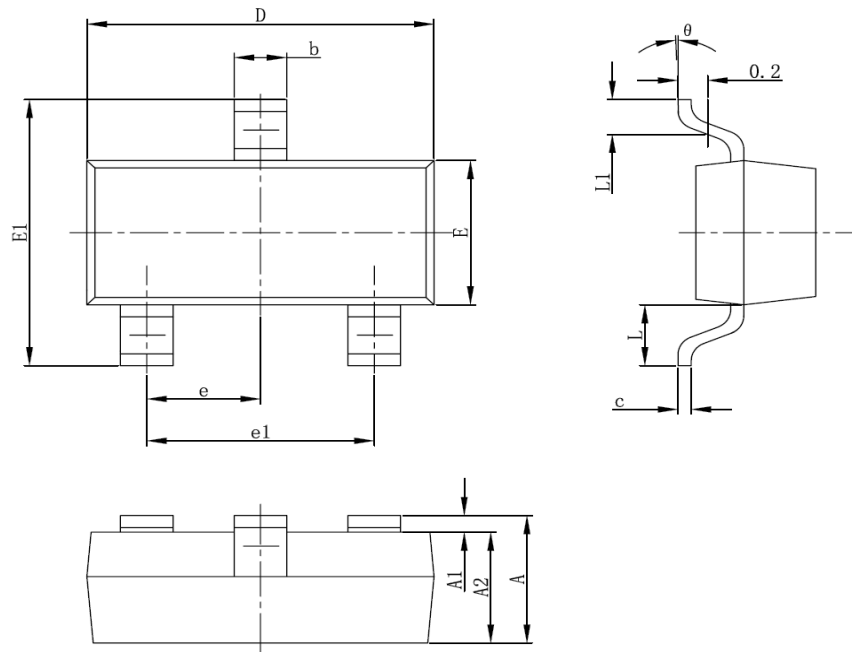
**Switching Times Test Circuit**



**Gate Charge Test Circuit**



**Test Circuit For Inductive Load  
Switching and Diode Recovery Times**

**SOT-23 PACKAGE OUTLINE**


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.550REF		0.022REF	
L1	0.300	0.500	0.012	0.020
$\theta$	0°	8°	0°	8°