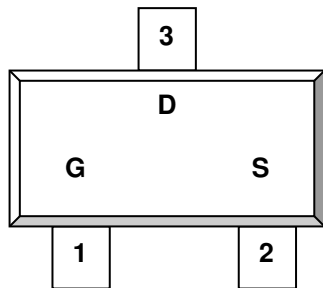


DESCRIPTION

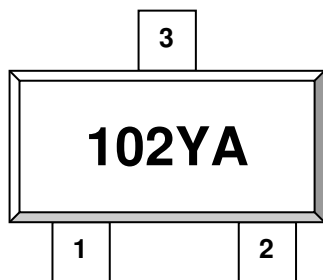
The ST1002 is the N-Channel logic enhancement mode power field effect transistor is produce using high cell density, DMOS trench technology. This high-density process is especially tailored to minimize on-state resistance. These device are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high side switching.

**PIN CONFIGURATION
SOT-23-3L**


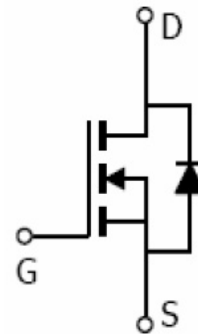
1.Gate 2.Source 3.Drain

FEATURE

- 100V/3.0A, $R_{DS(ON)} = 135m\Omega$
@ $V_{GS} = 10V$
- 100V/2.5A, $R_{DS(ON)} = 140m\Omega$
@ $V_{GS} = 4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23-3L package design

**PART MARKING
SOT-23-3L**


Y: Year Code A: Produce Code



**ST1002**

N Channel Enhancement Mode MOSFET

3.0A**ABSOLUTE MAXIMUM RATINGS** (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	100	V
Gate-Source Voltage	V _{GSS}	±20	V
Continuous Drain Current T _J =150°C	I _D	T _A =25°C 5.0	A
		T _A =70°C 3.0	
Pulsed Drain Current	I _{DM}	15	A
Continuous Source Current (Diode Conduction)	I _S	1.9	A
Power Dissipation	P _D	T _A =25°C 2.0	W
		T _A =70°C 1.2	
Operation Junction Temperature	T _J	-55/150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient	R _{θJA}	75	°C/W

ELECTRICAL CHARACTERISTICS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit	
Static							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	100			V	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1		2.5	V	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=80V, V_{GS}=0V$			1	uA	
		$V_{DS}=80V, V_{GS}=0V$ $T_J=55^\circ C$			10		
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=3.0A$ $V_{GS}=4.5V, I_D=2.0A$		128 133	135 140	m Ω	
Diode Forward Voltage	V_{SD}	$I_S=1.7A, V_{GS}=0V$			1.0	V	
Dynamic							
Total Gate Charge	Q_g	$V_{DS}=50V$ $V_{GS}=10V$ $I_D=2.0A$			45	nC	
Gate-Source Charge	Q_{gs}				7.2		
Gate-Drain Charge	Q_{gd}				22		
Input Capacitance	C_{iss}	$V_{DS}=30V$ $V_{GS}=0V$ $F=1MHz$		640		pF	
Output Capacitance	C_{oss}			160			
Reverse Transfer Capacitance	C_{rss}			88			
Turn-On Time	$t_{d(on)tr}$	$V_{DD}=30V$ $R_L=30\Omega$ $I_D=1.0A$ $V_{GEN}=10V$ $R_G=6\Omega$		11	21	nS	
Turn-Off Time	$t_{d(off)tf}$				10		19
					24		44
					21		39

TYPICAL CHARACTERISTICS (25°C Unless noted)

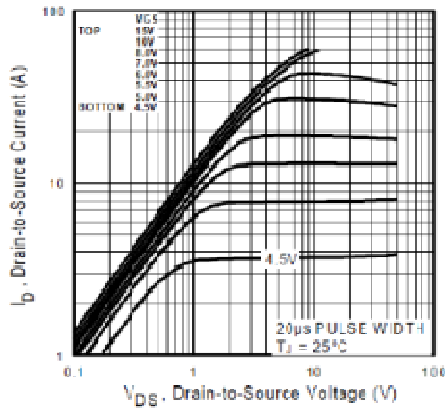


Fig 1. Typical Output Characteristics

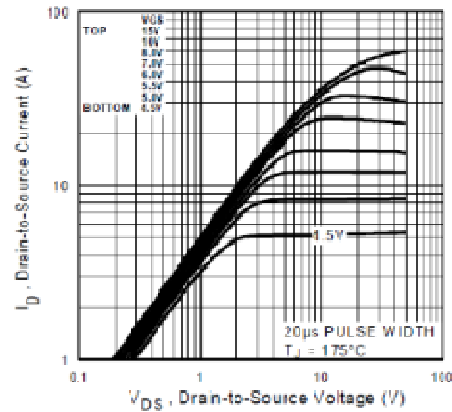


Fig 2. Typical Output Characteristics

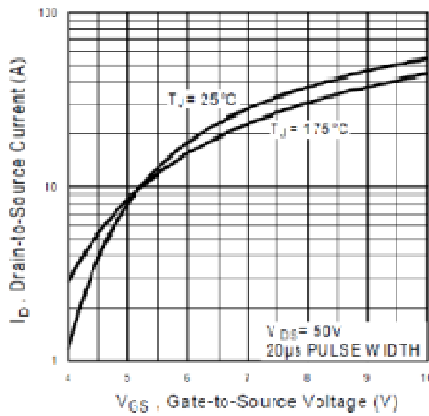


Fig 3. Typical Transfer Characteristics

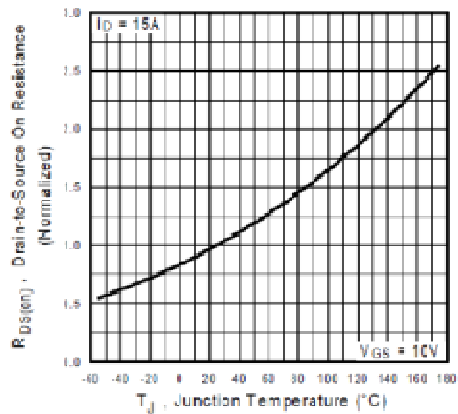
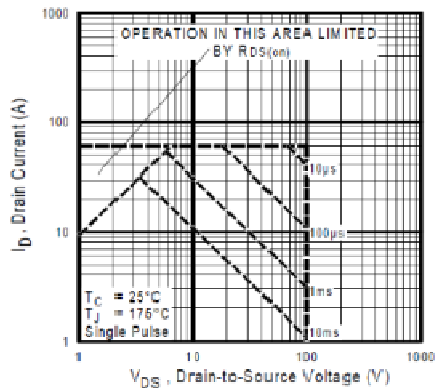
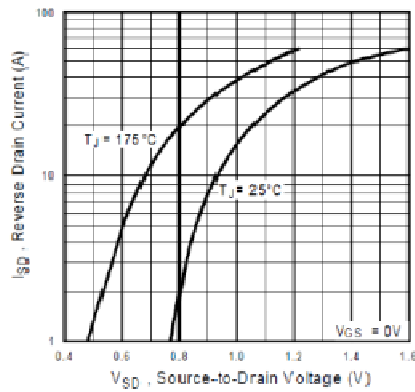
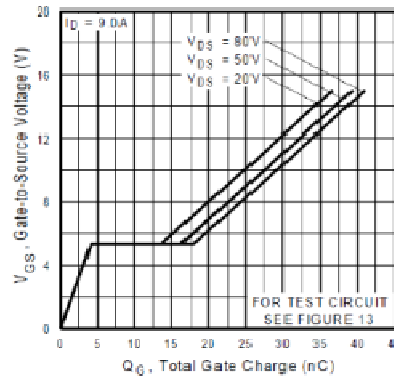
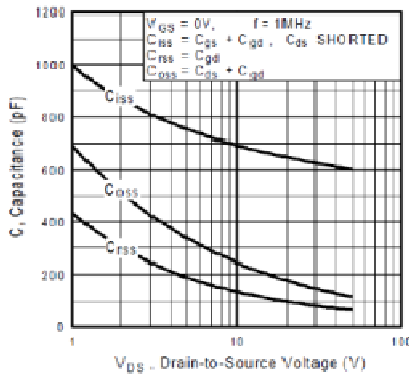


Fig 4. Normalized On-Resistance Vs. Temperature

TYPICAL CHARACTERISTICS (25°C Unless noted)



TYPICAL CHARACTERISTICS (25°C Unless noted)

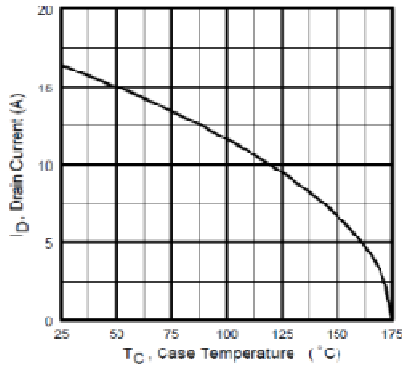


Fig 9. Maximum Drain Current Vs. Case Temperature

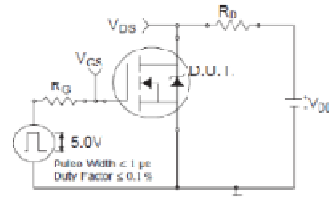


Fig 10a. Switching Time Test Circuit

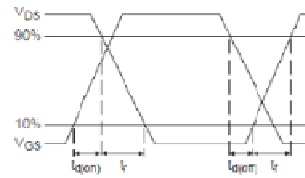


Fig 10b. Switching Time Waveforms

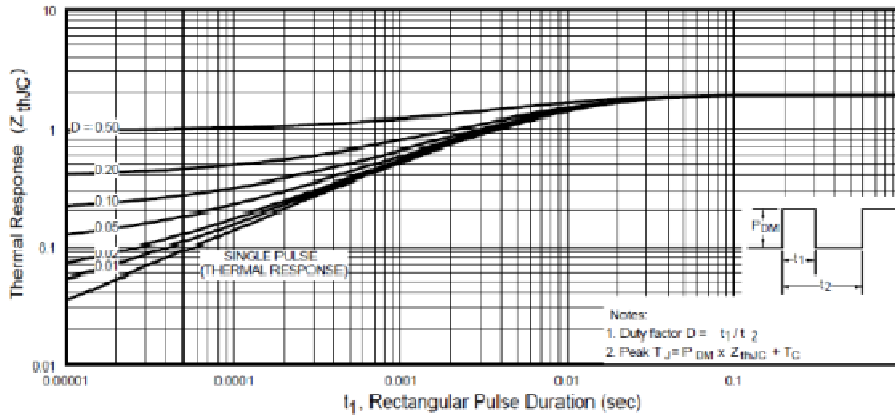
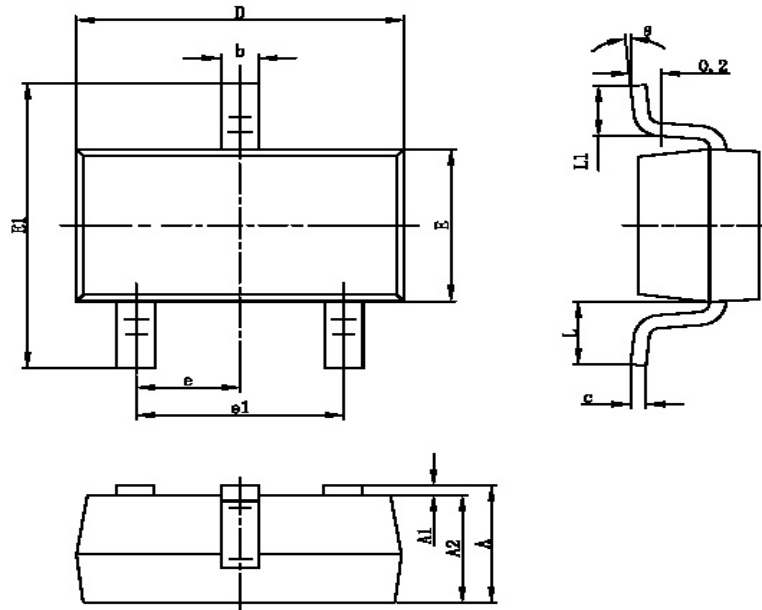


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

SOT-23-3L PACKAGE OUTLINE


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°