# ST05N20

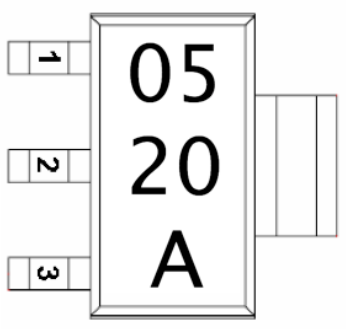
N Channel Enhancement Mode MOSFET

2.0A

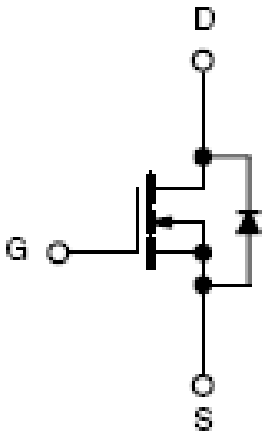
## DESCRIPTION

ST05N20 is the N-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as power management and other battery powered circuits where high-side switching.

## PIN CONFIGURATION
## SOT-223




**0520 : Product Code**
**A : Date Code**




## FEATURE

- 200V/2.0A, $R_{DS(ON)}$ = 800m @$V_{GS}$ = 10V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-223 package design

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**ABSOULTE MAXIMUM RATINGS** (Ta = 25℃ Unless otherwise noted )

| Parameter | | Symbol | Typical | Unit |
|---|---|---|---|---|
| Drain-Source Voltage | | VDSS | 200 | V |
| Gate-Source Voltage | | VGSS | ±30 | V |
| Continuous Drain Current (TJ=150℃) | TA=25℃<br>TA=100℃ | ID | 2<br>0.8 | A |
| Pulsed Drain Current | | IDM | 10 | A |
| Repetitive Avalanche Current | | EAS | 4.2 | mJ |
| Power Dissipation | TA=25℃ | PD | 1.78 | W |
| Operation Junction Temperature | | TJ | -55/150 | ℃ |
| Storgae Temperature Range | | TSTG | -55/150 | ℃ |
| Thermal Resistance-Junction to Ambient | | RθJA | 75 | ℃/W |

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**ELECTRICAL CHARACTERISTICS** ( Ta = 25℃ Unless otherwise noted )

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$=0V,ID=250uA | 200 | | | V |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$=$V_{GS}$,ID=250uA | 3 | 4 | 5 | V |
| Gate Leakage Current | $I_{GSS}$ | $V_{DS}$=0V,$V_{GS}$=±30V | | | ±100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$=160V,$V_{GS}$=0V | | | 1 | uA |
| Drain-source On-Resistance | $R_{DS(on)}$ | $V_{GS}$=10V,$I_D$=12A | | 750 | 800 | mΩ |
| Forward Transconductance | gfs | $V_{DS}$=10V,$I_D$=2A | | 3.6 | | S |
| Diode Forward Voltage | $V_{SD}$ | $I_S$=1A,$V_{GS}$=0V | | | 1 | V |
| **Dynamic** | | | | | | |
| Total Gate Charge | $Q_g$ | $V_{DS}$=160V,$V_{GS}$=10V $I_D$=1 A | | | 9 | nC |
| Gate-Source Charge | $Q_{gs}$ | | | | 4 | |
| Gate-Drain Charge | $Q_{gd}$ | | | | 2 | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ =25V,$V_{GS}$=0V f=1MHz | | 260 | 500 | pF |
| Output Capacitance | $C_{oss}$ | | | 160 | 300 | |
| Reverse TransferCapacitance | $C_{rss}$ | | | 55 | 110 | |
| Turn-On Time | $t_{d(on)}$ | $V_{DS}$=100 $V_{GEN}$=10V, $I_D$=1A $R_G$=25Ω | | 10 | 20 | nS |
| | tr | | | 35 | 70 | |
| Turn-Off Time | $t_{d(off)}$ | | | 10 | 20 | |
| | tf | | | 28 | 56 | |

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## TYPICAL CHATRCTERISTICS

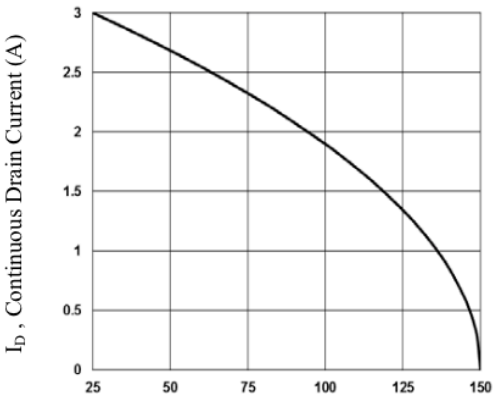


**Fig.1 Continuous Drain Current vs. $T_C$**

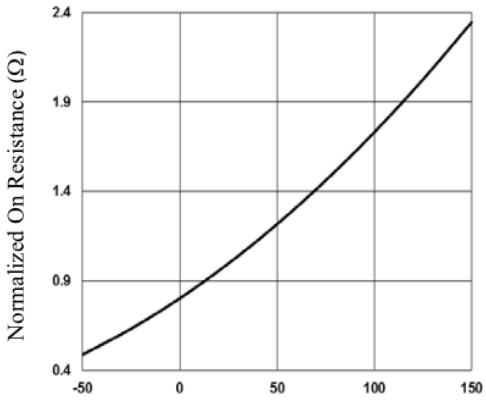


**Fig.2 Normalized RDSON vs. $T_J$**

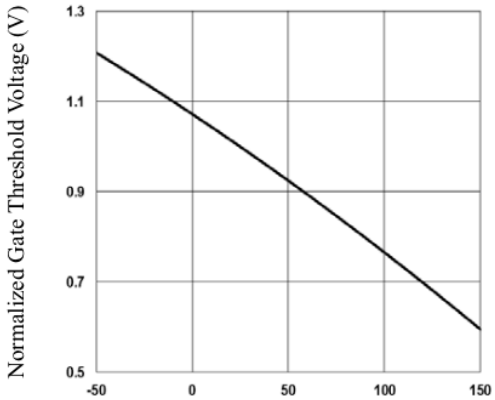


**Fig.3 Normalized $V_{th}$ vs. $T_J$**

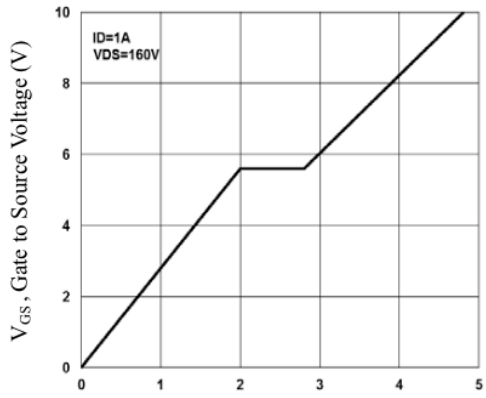


**Fig.4 Gate Charge Waveform**

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## TYPICAL CHATRCTERISTICS

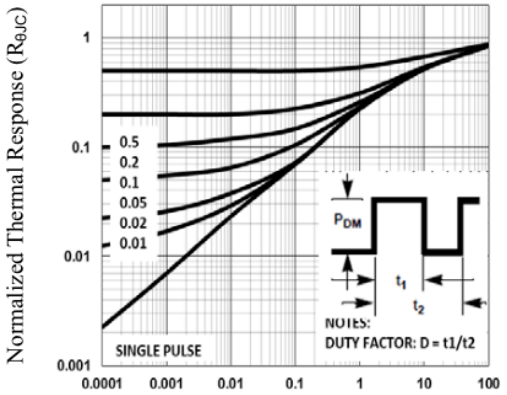


**Fig.5 Normalized Transient Impedance**

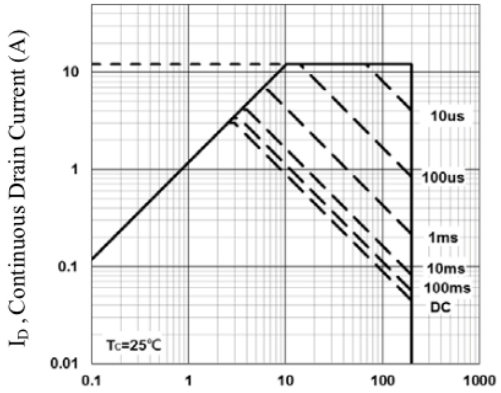


**Fig.6 Maximum Safe Operation Area**

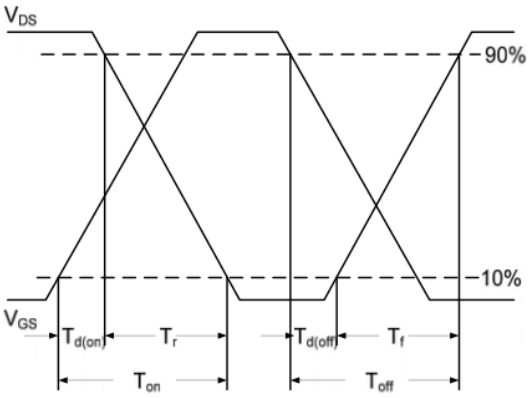


**Fig.7 Switching Time Waveform**

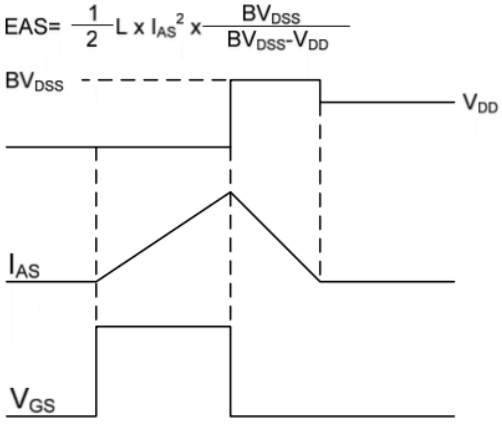


**Fig.8 EAS Waveform**

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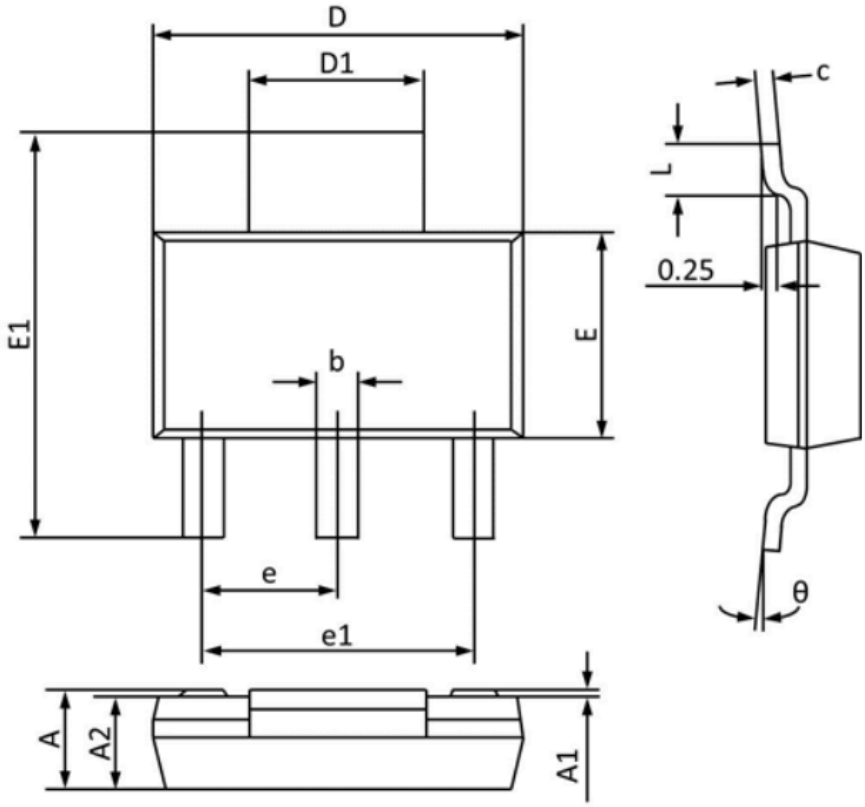
## PACKAGE OUTLINE SOT-223




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 1.520 | 1.800 | 0.060 | 0.071 |
| A1 | 0.000 | 0.100 | 0.000 | 0.004 |
| A2 | 1.500 | 1.700 | 0.059 | 0.067 |
| b | 0.660 | 0.820 | 0.026 | 0.032 |
| c | 0.250 | 0.350 | 0.010 | 0.014 |
| D | 6.200 | 6.400 | 0.244 | 0.252 |
| D1 | 2.900 | 3.100 | 0.114 | 0.122 |
| E | 3.300 | 3.700 | 0.130 | 0.146 |
| E1 | 6.830 | 7.070 | 0.269 | 0.278 |
| e | 2.300 (BSC) | | 0.091 (BSC) | |
| e1 | 4.500 | 4.700 | 0.177 | 0.185 |
| L | 0.900 | 1.150 | 0.035 | 0.045 |
| $\theta$ | 0° | 10° | 0° | 10° |

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