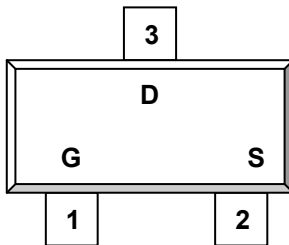
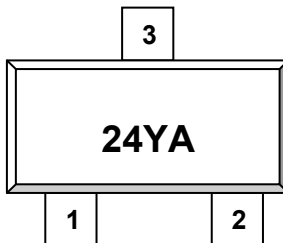


DESCRIPTION

ST1004SRG is the N-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. The process is especially to improve the overall efficiency of DC/DC conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(on)}$ and fast switching speed.

PIN CONFIGURATION
SOT-23


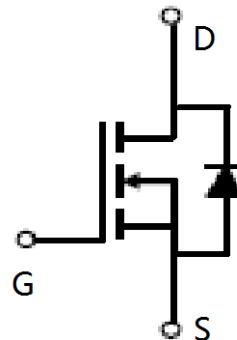
1.Gate 2.Source 3.Drain

PART MARKING
SOT-23


Y: Year Code A: Process Code

FEATURE

- 100V/1.0A, $R_{DS(ON)} = 310m\Omega$
@VGS = 10V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23 package design



**ST1004SRG**

N Channel Enhancement Mode MOSFET

2.0A**ABSOLUTE MAXIMUM RATINGS** (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	100	V
Gate-Source Voltage	V _{GSS}	±20	V
Continuous Drain Current=(150°C)	I _D	3.0 2.0	A
		T _A =25°C T _A =70°C	
Pulsed Drain Current	I _{DM}	10	A
Power Dissipation	P _D	1.25 0.8	W
		T _A =25°C T _A =70°C	
Operation Junction Temperature	T _J	150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient	R _{θJA}	100	°C/W



ST1004SRG



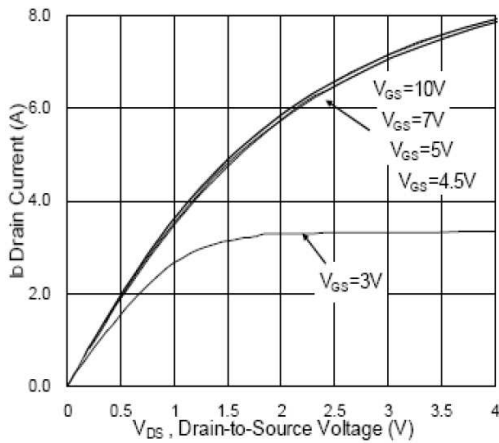
N Channel Enhancement Mode MOSFET

2.0A

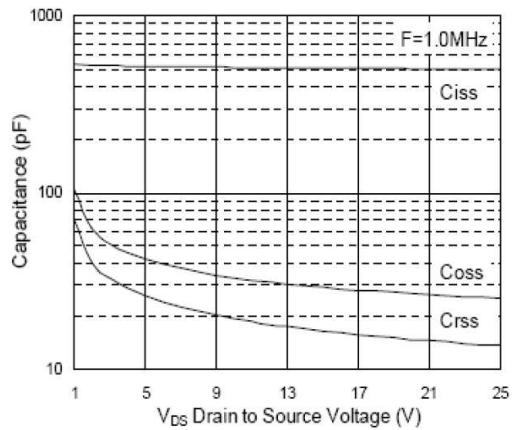
ELECTRICAL CHARACTERISTICS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0		2.5	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=80V, V_{GS}=0V$			1	uA
		$V_{DS}=80V, V_{GS}=0V$ $T_J=125^\circ C$			5	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \geq 5V, V_{GS}=10V$	3.0			A
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=2.0A$		0.26	0.31	Ω
		$V_{GS}=4.5V, I_D=1.0A$		0.29	0.32	
Forward Transconductance	g_{fs}	$V_{DS}=5V, I_D=3.6V$		2.4		S
Diode Forward Voltage	V_{SD}	$I_S=1.0A, V_{GS}=0V$			1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=80V$ $V_{GS}=10V$ $I_D=5.0A$		9	13	nC
Gate-Source Charge	Q_{gs}			2		
Gate-Drain Charge	Q_{gd}			1.4		
Input Capacitance	C_{iss}	$V_{DS}=25V$ $V_{GS}=0V$ $F=1MHz$		508		pF
Output Capacitance	C_{oss}			29		
Reverse Transfer Capacitance	C_{rss}			16.5		
Turn-On Time	$t_{d(on)tr}$	$V_{DD}=50V$ $R_L=10\Omega$ $I_D=3.0A$ $V_{GEN}=10V$ $R_G=3.3\Omega$		12		nS
				21.5		
Turn-Off Time	$t_{d(off)tf}$			11.2		
				18.8		

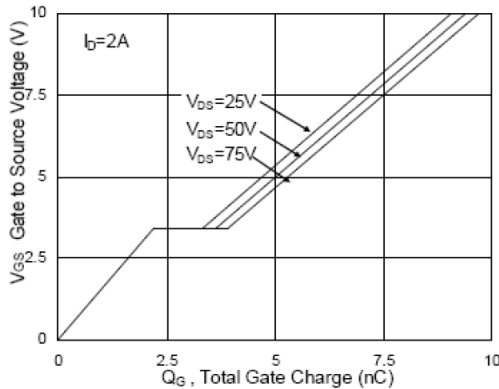
TYPICAL CHARACTERISTICS (25°C Unless noted)



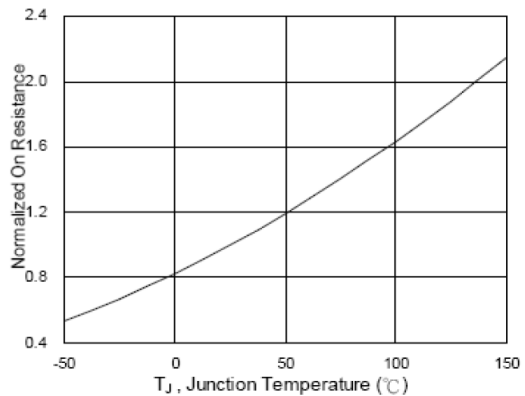
Output Characteristics



Capacitance

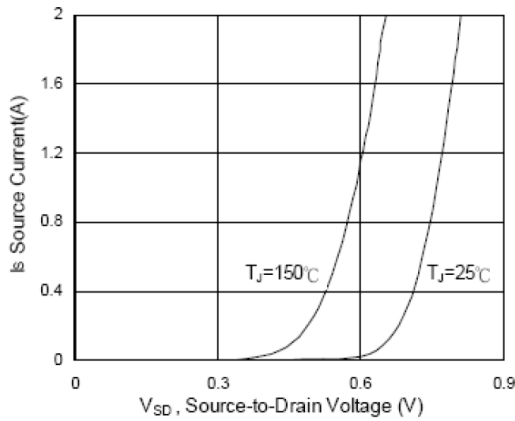


Gate Charge

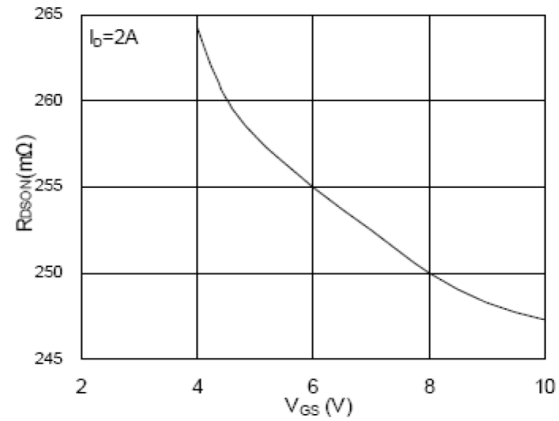


On-Resistance vs. Junction Temperature

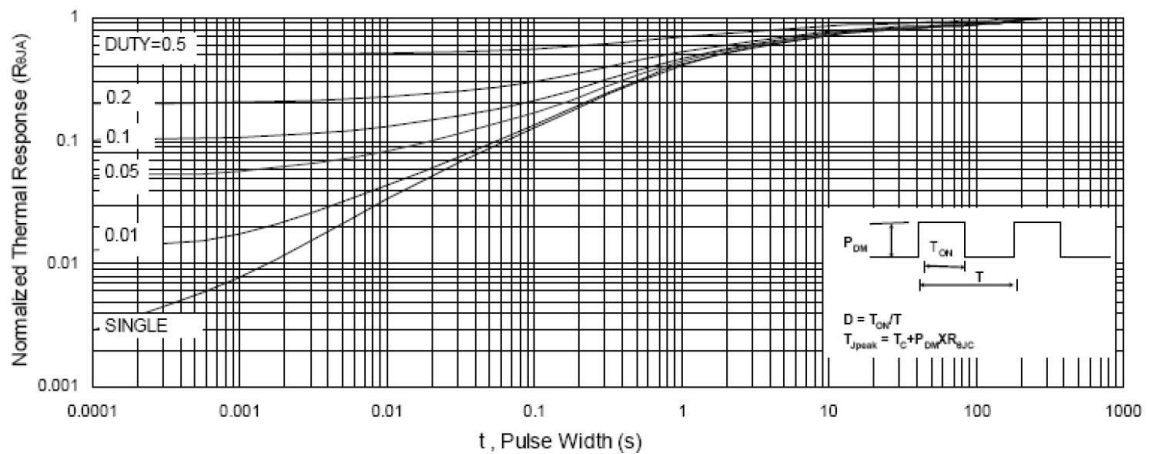
TYPICAL CHARACTERISTICS (25°C Unless noted)



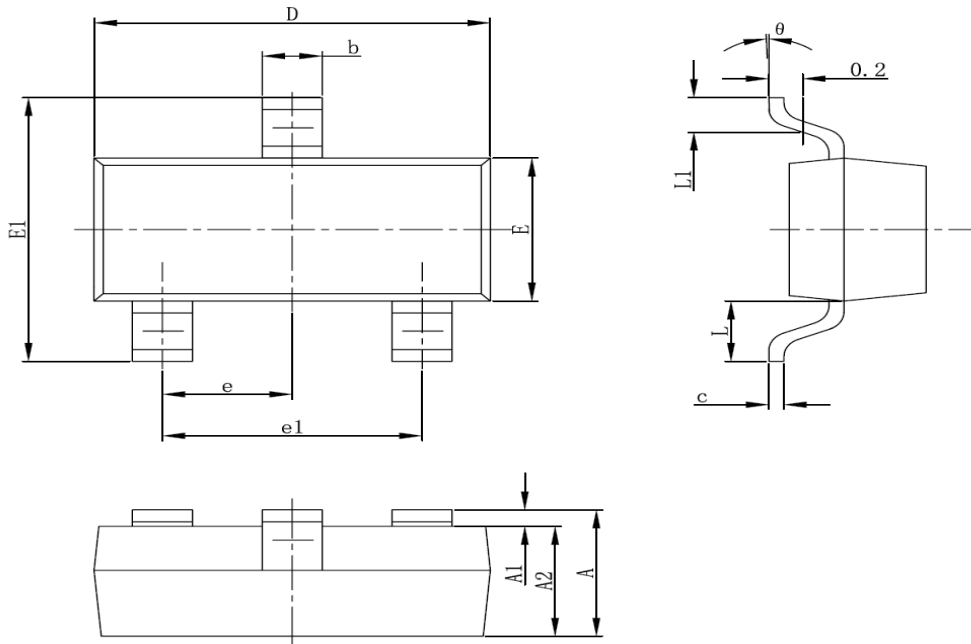
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-Source Voltage



Normalized Thermal Transient Impedance, Junction to Foot

SOT-23 PACKAGE OUTLINE


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.550REF		0.022REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°