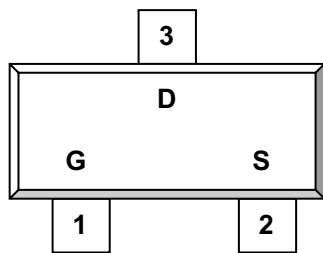
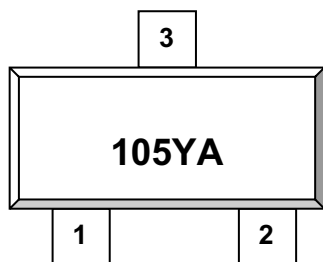


**DESCRIPTION**

ST1005SRG is the P-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management, other battery powered circuits, and low in-line power loss are required. The product is in a very small outline surface mount package.

**PIN CONFIGURATION  
SOT-23**


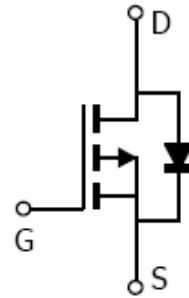
1.Gate 2.Source 3.Drain

**PART MARKING  
SOT-23**


Y: Year Code A: Process Code

**FEATURE**

- -100V/-0.8A,  $R_{DS(ON)} = 650\text{m-ohm (Typ.)}$   
@VGS = -10V
- -100V/-0.4A,  $R_{DS(ON)} = 700\text{m-ohm}$   
@VGS = -4.5V
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23 package design



**ST1005SRG**

P Channel Enhancement Mode MOSFET

**-0.8A****ABSOLUTE MAXIMUM RATINGS** (Ta = 25°C Unless otherwise noted )

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V <sub>DSS</sub>	-100	V
Gate-Source Voltage	V <sub>GSS</sub>	±20	V
Continuous Drain Current (T <sub>J</sub> =150°C)	I <sub>D</sub>	T <sub>A</sub> =25°C -0.8	A
		T <sub>A</sub> =70°C -0.4	
Pulsed Drain Current	I <sub>DM</sub>	-4	A
Continuous Source Current (Diode Conduction)	I <sub>S</sub>	-1.0	A
Power Dissipation	P <sub>D</sub>	T <sub>A</sub> =25°C 1.25	W
		T <sub>A</sub> =70°C 0.8	
Operation Junction Temperature	T <sub>J</sub>	150	°C
Storage Temperature Range	T <sub>STG</sub>	-55/150	°C
Thermal Resistance-Junction to Ambient	R <sub>θJA</sub>	85	°C/W



**ST1005SRG**



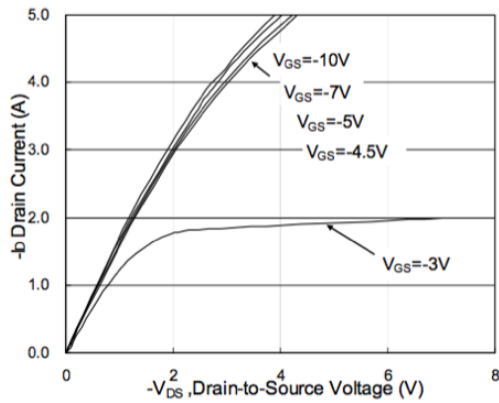
P Channel Enhancement Mode MOSFET

**-0.8A**

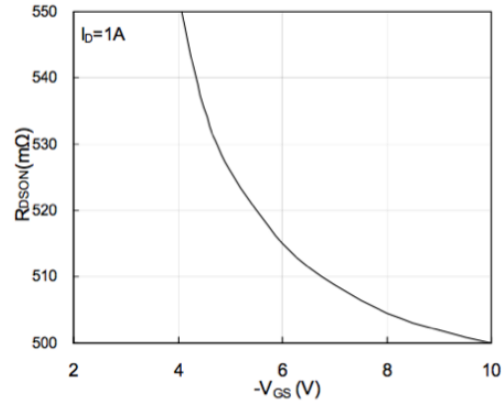
**ELECTRICAL CHARACTERISTICS** ( Ta = 25°C Unless otherwise noted )

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-10\mu A$	-100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.0		-2.5	V
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-80V, V_{GS}=0V$			-1	uA
		$V_{DS}=-80V, V_{GS}=0V$ $T_J=55^\circ C$			-5	
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-0.8A$ $V_{GS}=-4.5V, I_D=-0.4A$		0.640 0.690	0.650 0.700	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS}=-5V, I_D=-0.8A$		2.0		S
Diode Forward Voltage	$V_{SD}$	$I_S=-1.0A, V_{GS}=0V$			-0.8	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=-50V$ $V_{GS}=-10V$ $I_D \equiv -0.5A$		16		nC
Gate-Source Charge	$Q_{gs}$			9		
Gate-Drain Charge	$Q_{gd}$			1.23		
Input Capacitance	$C_{iss}$	$V_{DS}=-15V$ $V_{GS}=0V$ $F=1MHz$			600	pF
Output Capacitance	$C_{oss}$			550		
Reverse Transfer Capacitance	$C_{rss}$			20		
Turn-On Time	$t_{d(on)}$ $t_r$	$V_{DD}=-50V$ $I_D=-0.5A$ $V_{GS}=-10V$ $R_G=2.5\Omega$		2		nS
				19		
Turn-Off Time	$t_{d(off)}$ $t_f$			18.5		
				20		

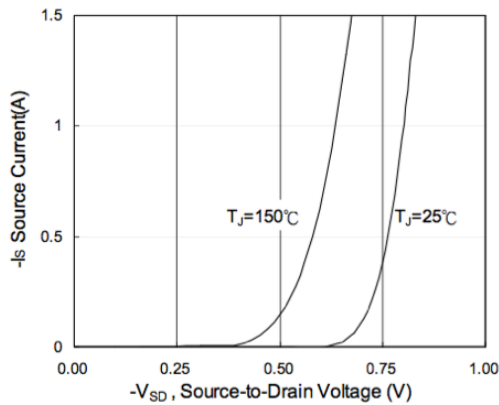
**TYPICAL CHARACTERISTICS**



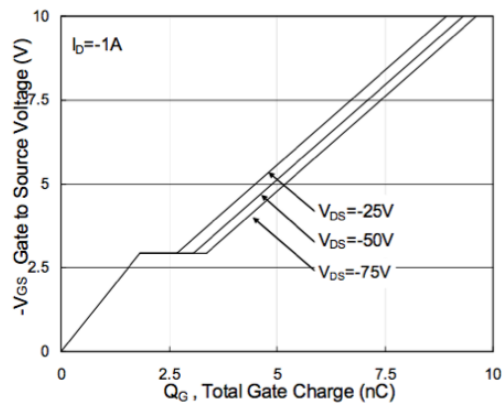
**Fig.1 Typical Output Characteristics**



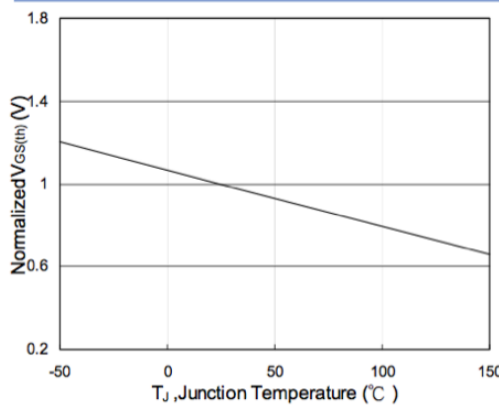
**Fig.2 On-Resistance vs. Gate-Source**



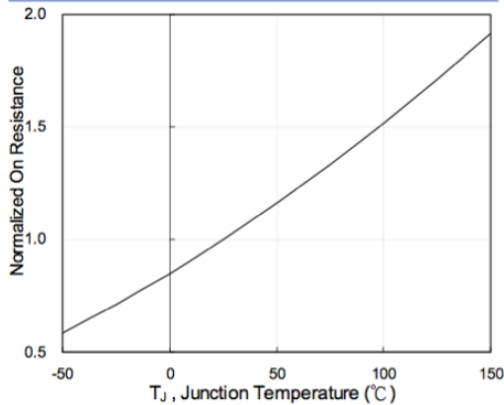
**Fig.3 Forward Characteristics Of Reverse**



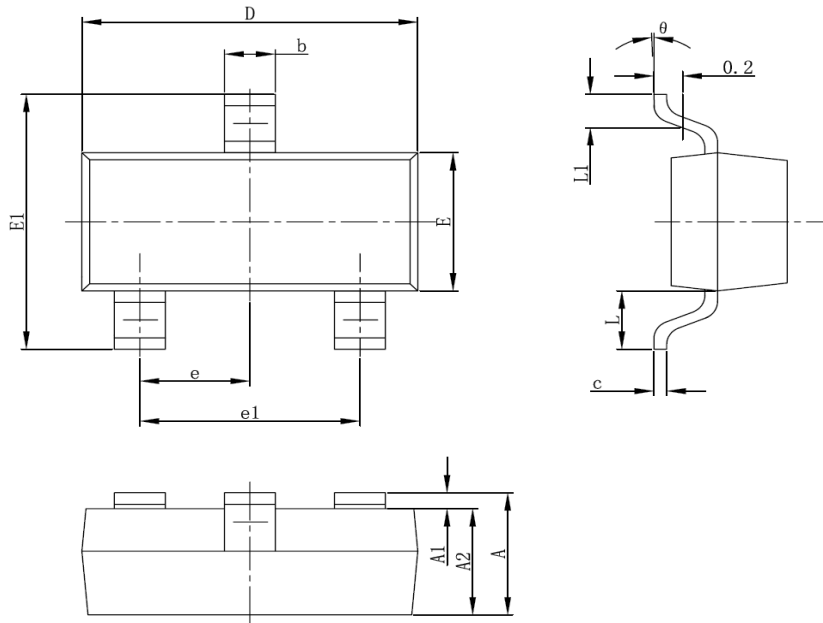
**Fig.4 Gate-Charge Characteristics**



**Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$**



**Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$**

**SOT-23 PACKAGE OUTLINE**


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.550REF		0.022REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°