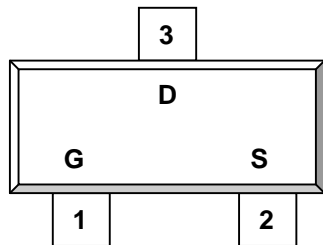


DESCRIPTION

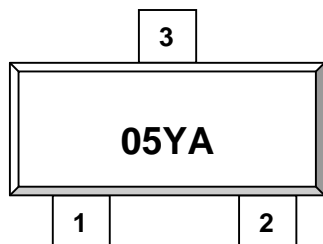
ST2005SRG is the P-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management, other battery powered circuits, and low in-line power loss are required. The product is in a very small outline surface mount package.

PIN CONFIGURATION
SOT-23


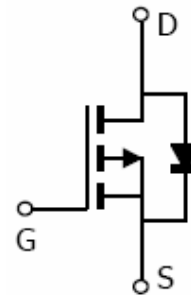
1.Gate 2.Source 3.Drain

FEATURE

- I -20V/-3.5A, $R_{DS(ON)} = 40\text{m-ohm}$ (Typ.) @VGS = -4.5V
- I -20V/-3.0A, $R_{DS(ON)} = 60\text{m-ohm}$ @VGS = -2.5V
- I -20V/-1.8A, $R_{DS(ON)} = 90\text{m-ohm}$ @VGS=-1.8V
- I Super high density cell design for extremely low $R_{DS(ON)}$
- I Exceptional on-resistance and maximum DC current capability
- I SOT-23 package design

PART MARKING
SOT-23


Y: Year Code A: Process Code


ORDERING INFORMATION

Part Number	Package	Part Marking
ST2005SRG	SOT-23	05YA

* Process Code : A ~ Z ; a ~ z

* ST2005SRG S : SOT23 ; R : Tape Reel ; G : Pb - Free

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ST2005SRG



P Channel Enhancement Mode MOSFET

-3.5A

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	-20	V
Gate-Source Voltage	V _{GSS}	±8	V
Continuous Drain Current (T _J =150°C)	I _D	T _A =25°C -3.5	A
		T _A =70°C -2.8	
Pulsed Drain Current	I _{DM}	-10	A
Continuous Source Current (Diode Conduction)	I _S	-1.6	A
Power Dissipation	P _D	T _A =25°C 1.25	W
		T _A =70°C 0.8	
Operation Junction Temperature	T _J	150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient	R _{θJA}	120	°C/W

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ST2005SRG



P Channel Enhancement Mode MOSFET

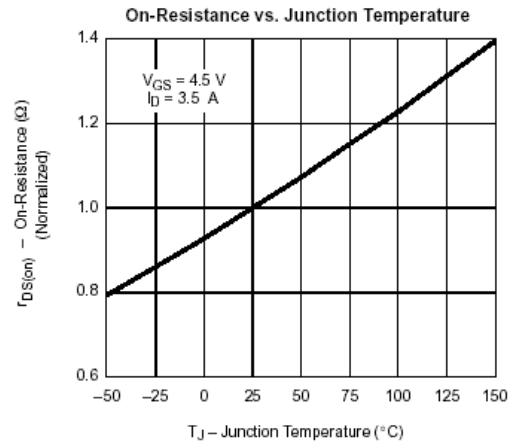
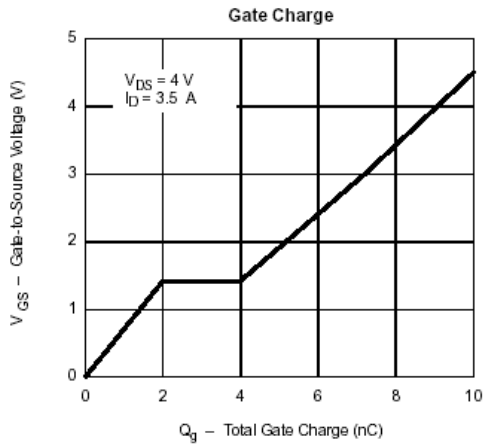
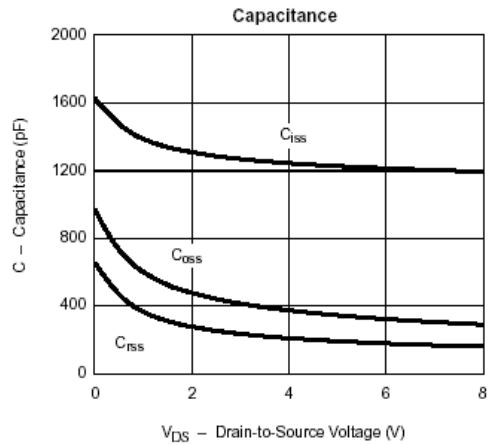
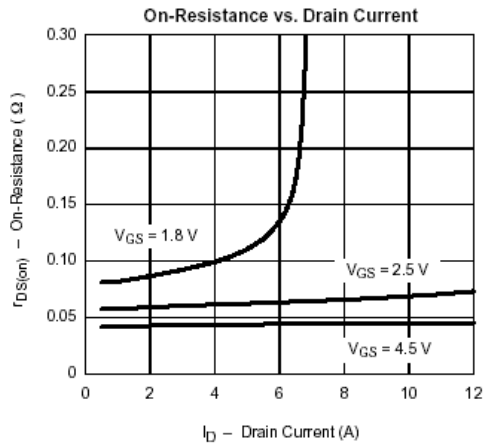
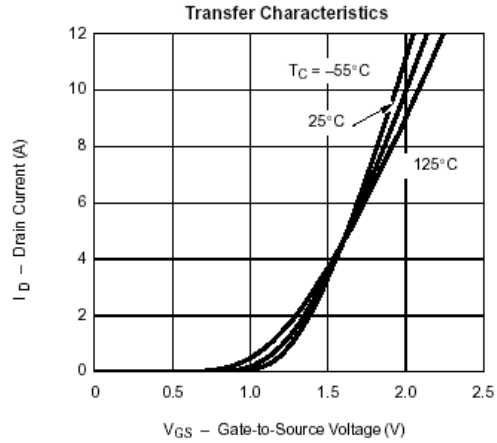
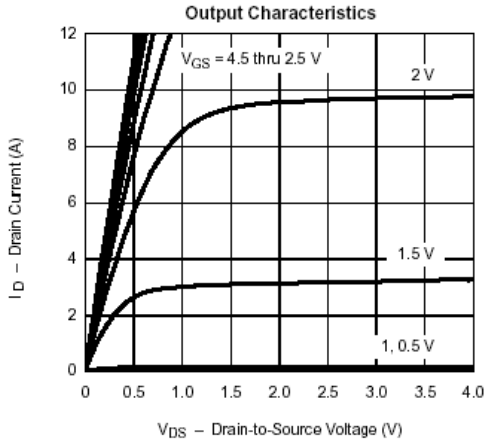
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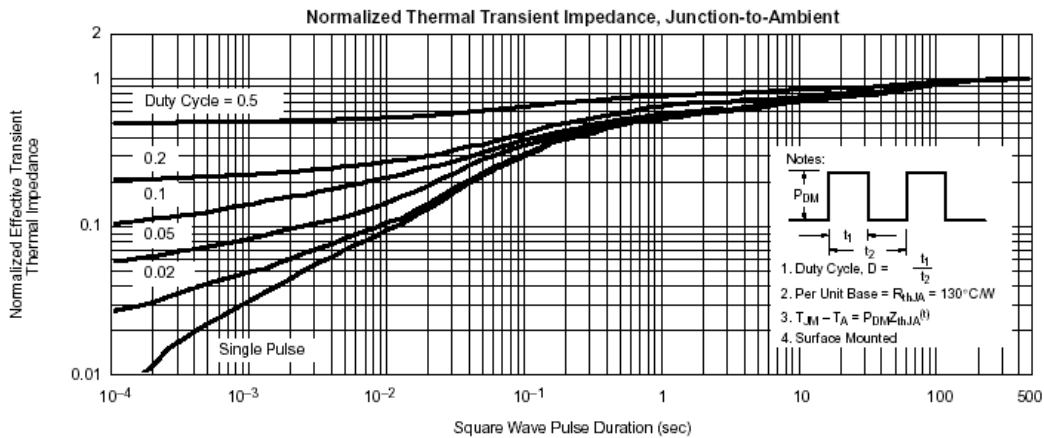
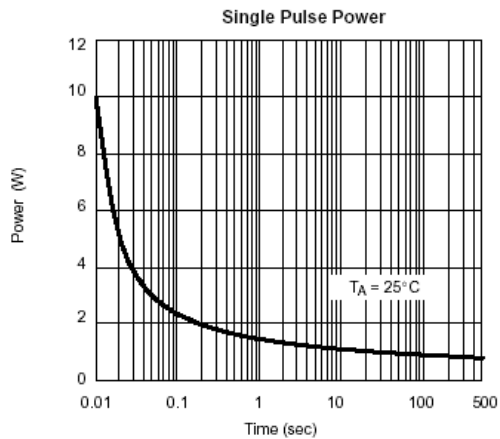
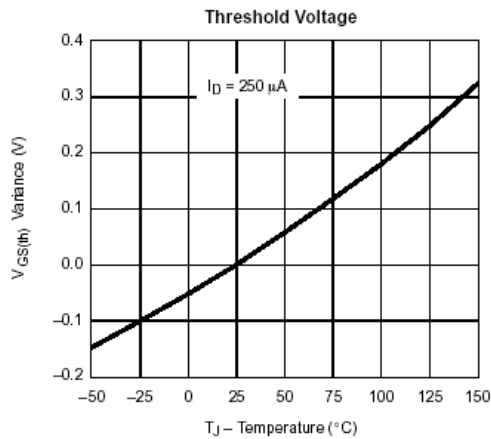
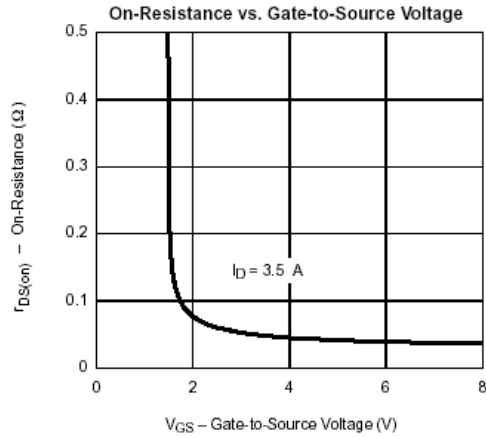
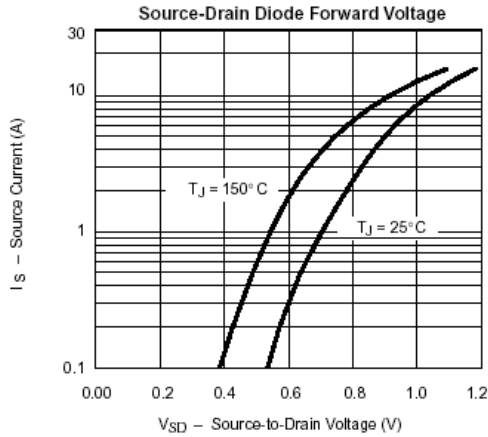
ELECTRICAL CHARACTERISTICS (Ta = 25°C Unless otherwise noted)

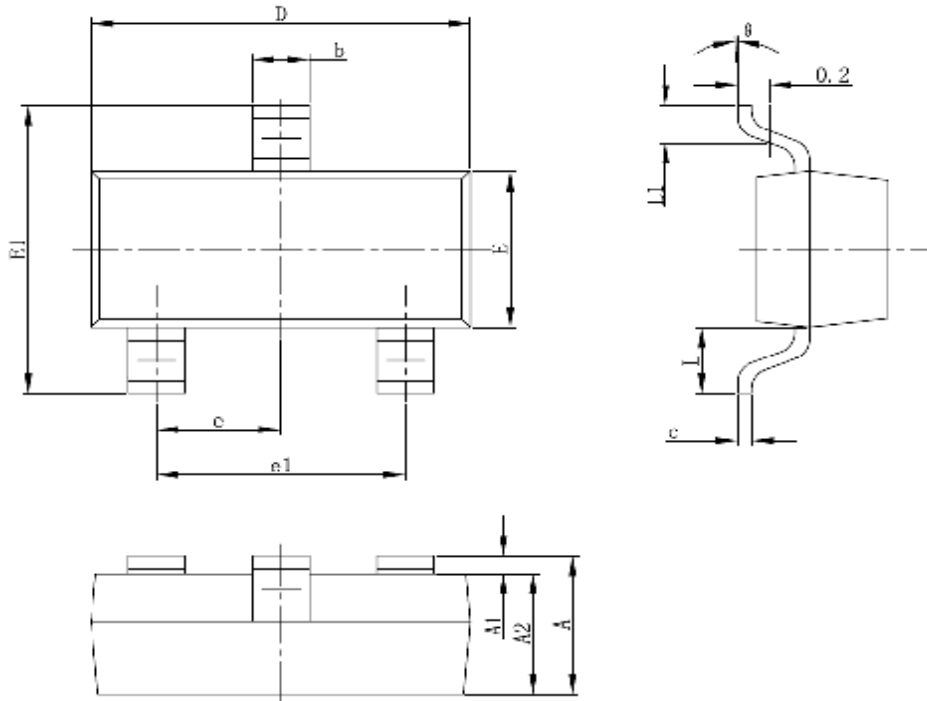
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-20			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.3		-1.0	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 8V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-20V, V_{GS}=0V$			-1	uA
		$V_{DS}=-20V, V_{GS}=0V$ $T_J=55^\circ C$			-10	
On-State Drain Current	$I_{D(on)}$	$V_{DS}\leq -5V, V_{GS}=-4.5V$	-6			A
		$V_{DS}\leq -5V, V_{GS}=-2.5V$	-3			
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-3.5A$		0.040	0.047	Ω
		$V_{GS}=-2.5V, I_D=-3.0A$		0.060	0.070	
		$V_{GS}=-1.8V, I_D=-2.0A$		0.090	0.099	
Forward Transconductance	g_{fs}	$V_{DS}=-5V, I_D=-3.5V$		8.5		S
Diode Forward Voltage	V_{SD}	$I_S=-1.6A, V_{GS}=0V$		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=-10V$ $V_{GS}=-4.5V$ $I_D=-3.5A$		10	12	nC
Gate-Source Charge	Q_{gs}			2		
Gate-Drain Charge	Q_{gd}			2		
Input Capacitance	C_{iss}	$V_{DS}=-10V$ $V_{GS}=0V$ $F=1MHz$		485		pF
Output Capacitance	C_{oss}			90		
Reverse Transfer Capacitance	C_{rss}			40		
Turn-On Time	$t_{d(on)}$ t_r	$V_{DD}=-10V$ $R_L=6\Omega$ $I_D=-1.0A$ $V_{GEN}=-4.5V$ $R_G=6\Omega$		10	18	nS
				13	22	
Turn-Off Time	$t_{d(off)}$ t_f			18	24	
				15	20	

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TYPICAL CHARACTERISTICS (25°C Unless noted)


TYPICAL CHARACTERISTICS (25°C Unless noted)


SOT-23 PACKAGE OUTLINE


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.550REF		0.022REF	
L1	0.300	0.500	0.012	0.020
theta	0°	8°	0°	8°