ST3413A

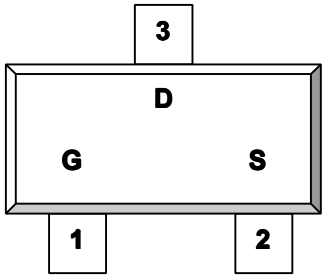
P Channel Enhancement Mode MOSFET

-3.5A

DESCRIPTION

ST3413A is the P-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management, other battery powered circuits, and low in-line power loss are required. The product is in a very small outline surface mount package.

PIN CONFIGURATION
SOT-23-3L

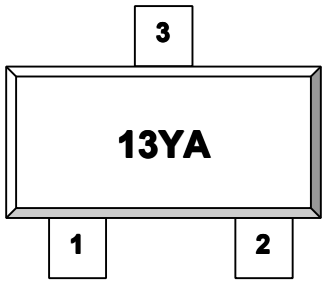


1.Gate 2.Source 3.Drain

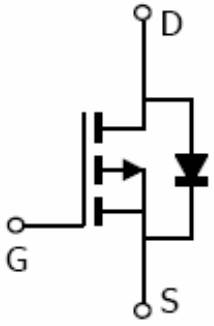
FEATURE

- -20V/-3.4A, $R_{DS(ON)}$ = 60mΩ (Typ.)
  @V_{GS} = -4.5V
- -20V/-2.4A, $R_{DS(ON)}$ = 80mΩ
  @V_{GS} = -2.5V
- -20V/-1.7A, $R_{DS(ON)}$ = 90mΩ
  @V_{GS} = -1.8V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23-3L package design

PART MARKING
SOT-23-3L



Y: Year Code A: Week Code



ORDERING INFORMATION

Part Number	Package	Part Marking
ST3413A	SOT-23	13YA

※ Week Code ： A ~ Z ; a ~ z

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ABSOULTE MAXIMUM RATINGS (Ta = 25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	-20	V
Gate-Source Voltage		V_{GSS}	±12	V
Continuous Drain Current (TJ=150℃)	T_A=25℃ T_A=70℃	I_D	-3.5 -2.8	A
Pulsed Drain Current		I_{DM}	-15	A
Continuous Source Current (Diode Conduction)		I_S	-1.4	A
Power Dissipation	T_A=25℃ T_A=70℃	P_D	1.25 0.8	W
Operation Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	105	℃/W

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ELECTRICAL CHARACTERISTICS (Ta = 25℃ Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=-250uA	-20			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=VGS,I_D=-250uA	-0.35		-0.8	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±12V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-20V,V_{GS}=0V			-1	uA
		V_{DS}=-20V,V_{GS}=0V T_J=55℃			-5	
On-State Drain Current	$I_{D(on)}$	V_{DS}≦-5V,V_{GS}=-4.5V V_{DS}≦-5V,V_{GS}=-2.5V	-6 -3			A
Drain-source On-Resistance	$R_{DS(on)}$	V_{GS}=-1.8V,I_D=-1.7A V_{GS}=-2.5V,I_D=-2.4A V_{GS}=-4.5V,I_D=-3.4A		0.090 0.080 0.060		Ω
Forward Transconductance	g_{fs}	V_{DS}=-5V,I_D=-2.8A		6		S
Diode Forward Voltage	V_{SD}	I_S=-1.5A,V_{GS}=0V		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=-6V V_{GS}=-4.5V I_D=-2.8A		4.8	8	nC
Gate-Source Charge	Q_{gs}			1.0		
Gate-Drain Charge	Q_{gd}			1.0		
Input Capacitance	C_{iss}	V_{DS}=-6V V_{GS}=0V f=1MHz		485		pF
Output Capacitance	C_{oss}			85		
Reverse Transfer Capacitance	C_{rss}			40		
Turn-On Time	$t_{d(on)}$ tr	V_{DD}=-6V R_L=6Ω I_D=-1A V_{GEN}=-4.5V R_G=6Ω		10	16	nS
				13	23	
Turn-Off Time	$t_{d(off)}$ tf			18	25	
				15	20	

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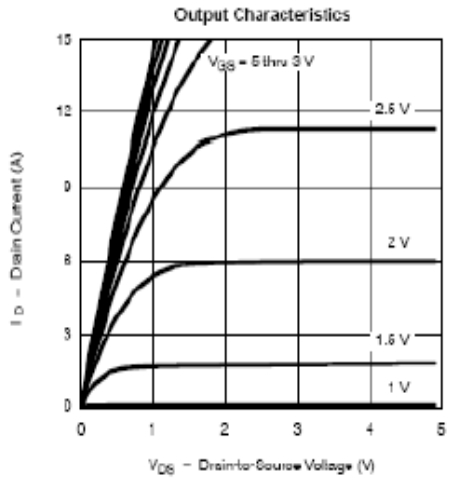
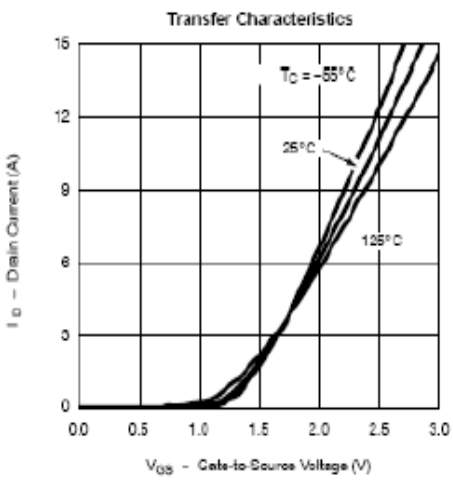
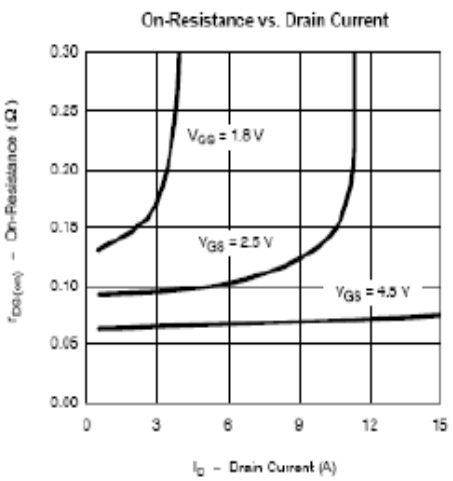
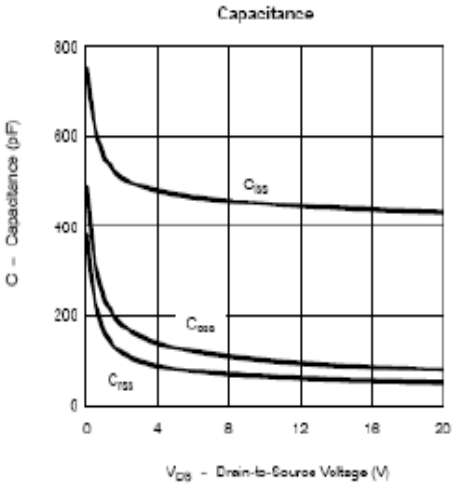
TYPICAL CHARACTERICTICS (25℃ Unless noted)









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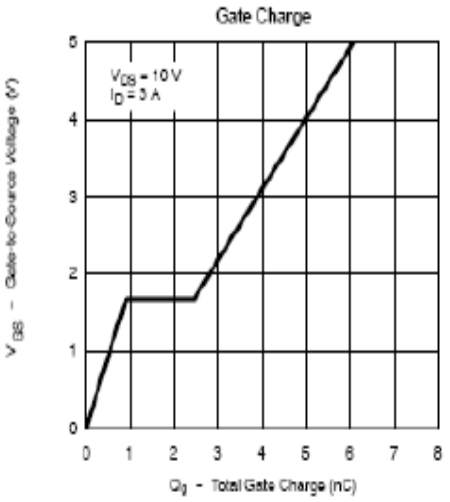

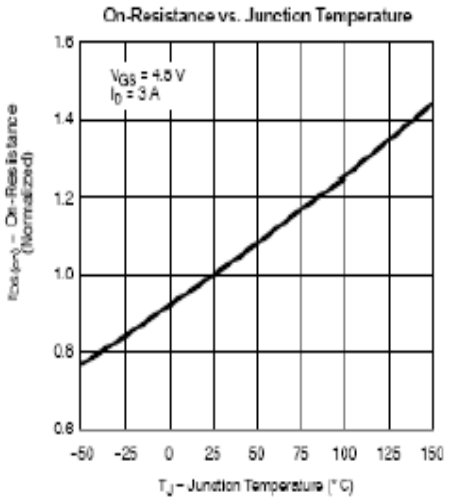

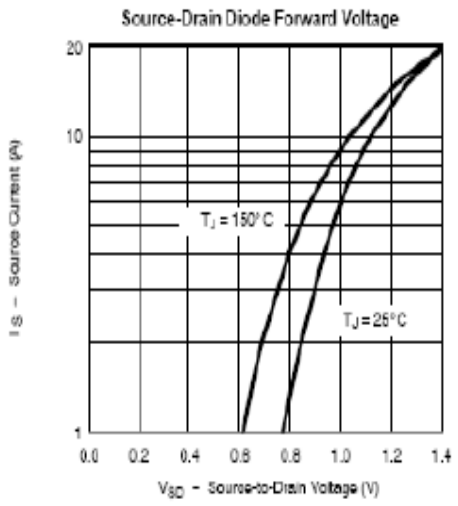

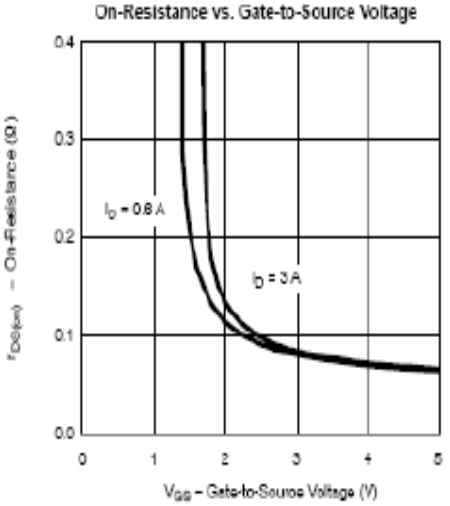

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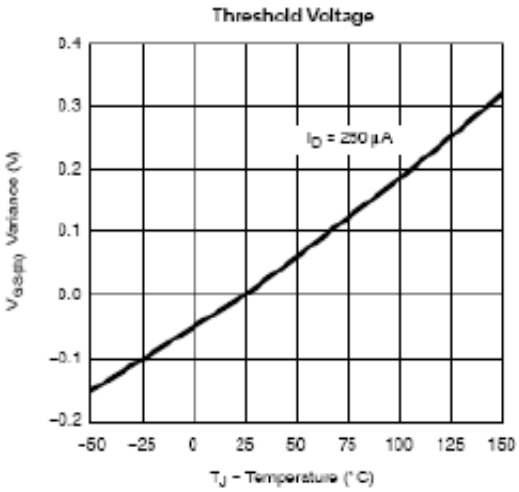

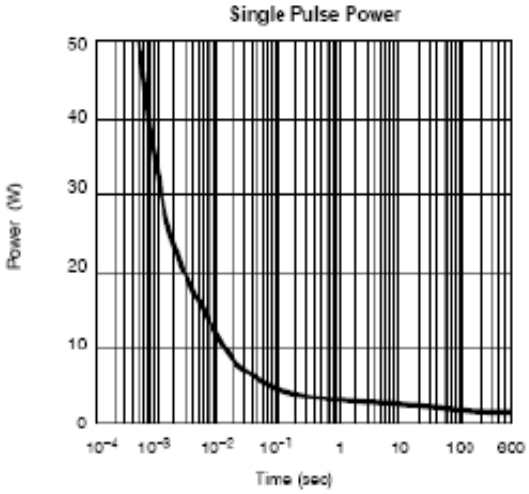

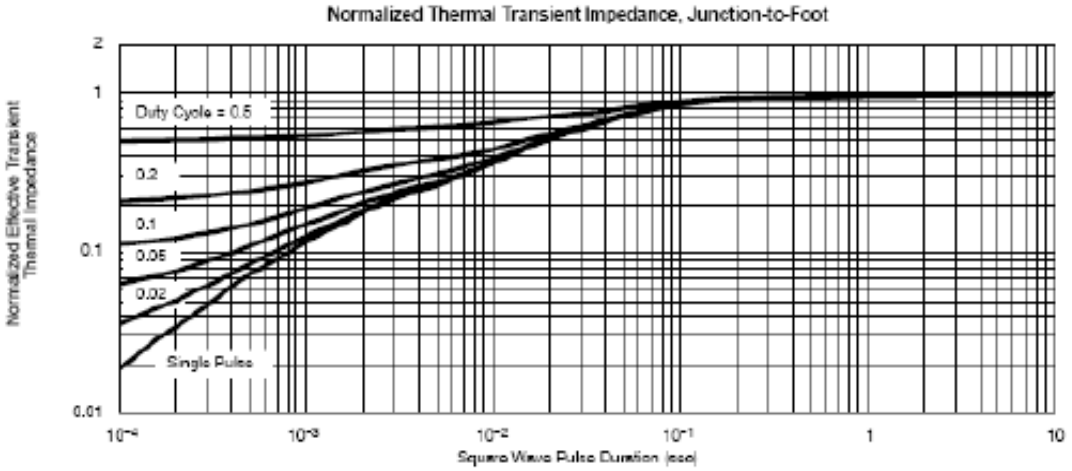

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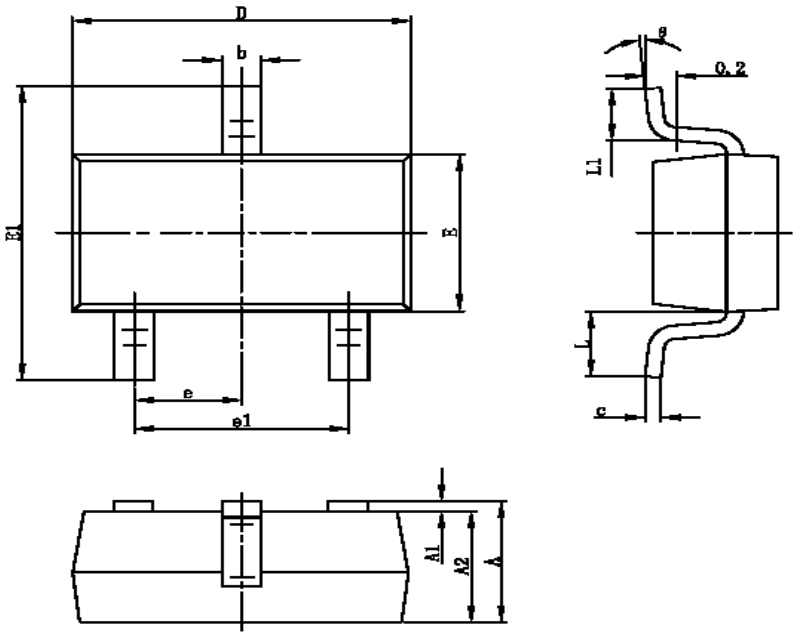
SOT-23-3L PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

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