



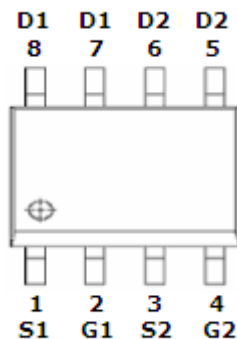
STN4972 

Dual N Channel Enhancement Mode MOSFET
8.5A

DESCRIPTION

STN4972 is the Dual N-Channel logic enhancement mode power field effect transistors which are produced using high cell density DMOS trench technology. It is suitable for the power management applications in the portable or battery powered system.

PIN CONFIGURATION SOP-8



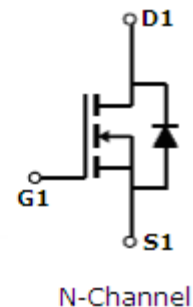
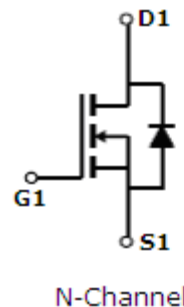
FEATURE

- 30V/8.5A, $R_{DS(ON)} = 14m\Omega @ V_{GS} = 10V$
- 30V/7.8A, $R_{DS(ON)} = 18m\Omega @ V_{GS} = 4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOP-8 package design

PART MARKING SOP-8



S : Subcontractor Y : Year Code
A : Process Code



ORDERING INFORMATION

Part Number	Package	Part Marking
STN4972S8RG	SOP-8	STN4972
STN4972S8TG	SOP-8	STN4972

※ Process Code : A ~ Z ; a ~ z

※ STN9972S8RG S8 : SOP-8 ; R : Tape Reel ; G : Pb – Free

※ STN9972S8TG S8 : SOP-8 ; T : Tube ; G : Pb – Free

STANSON TECHNOLOGY
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**STN4972**Dual N Channel Enhancement Mode MOSFET
8.5A**ABSOLUTE MAXIMUM RATINGS** (Ta = 25°C Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V _{DSS}	30	V
Gate-Source Voltage		V _{GSS}	±20	V
Continuous Drain Current (T _J =150°C)	T _A =25°C T _A =70°C	I _D	8.5 7.5	A
Pulsed Drain Current		I _{DM}	25	A
Continuous Source Current (Diode Conduction)		I _S	2.3	A
Power Dissipation	T _A =25°C T _A =70°C	P _D	2.5 1.6	W
Operation Junction Temperature		T _J	-55/150	°C
Storage Temperature Range		T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient		R _{θJA}	80	°C/W



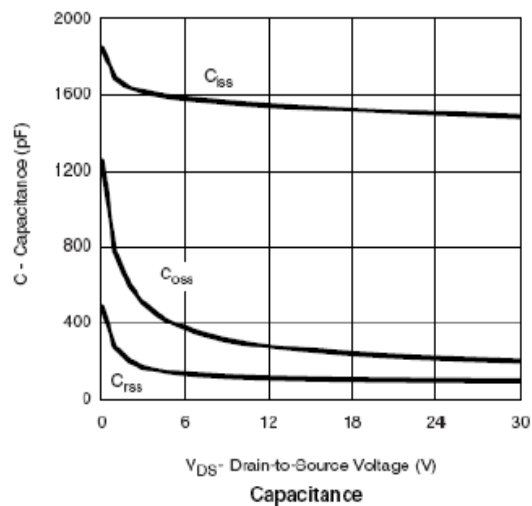
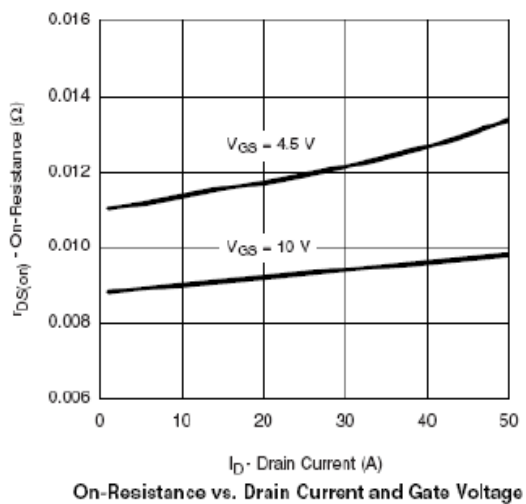
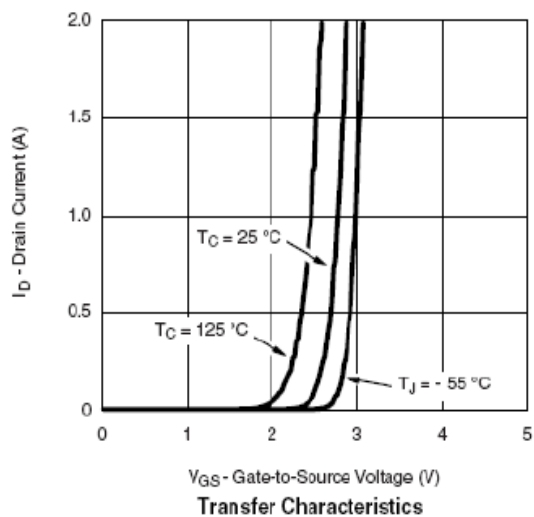
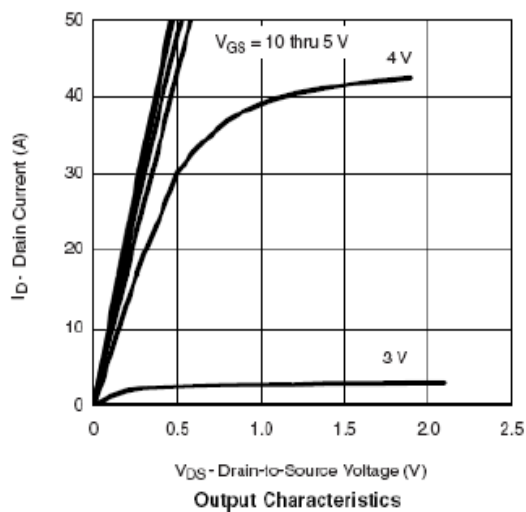
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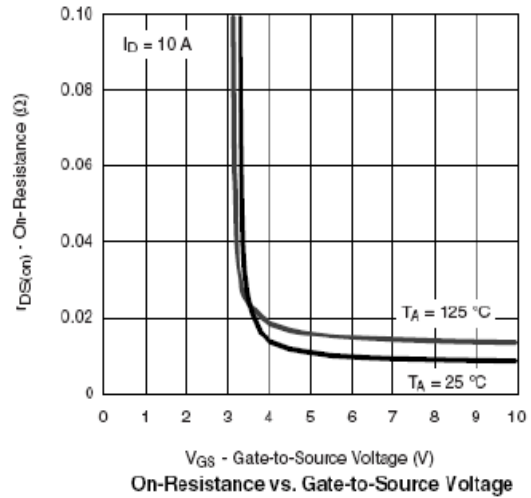
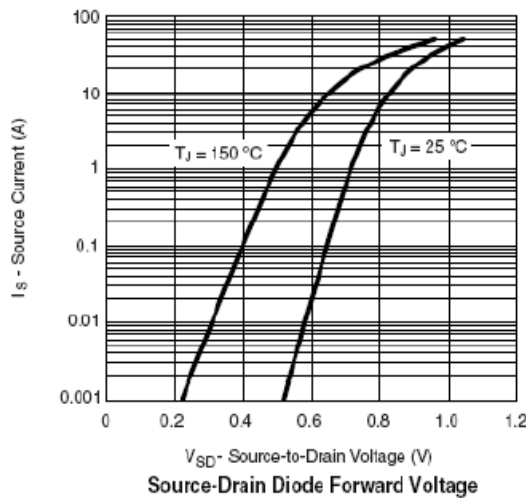
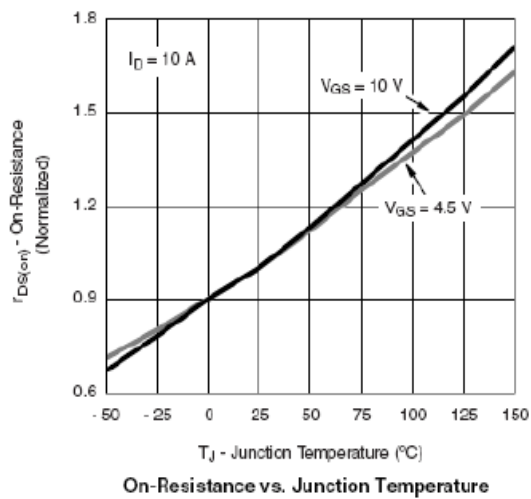
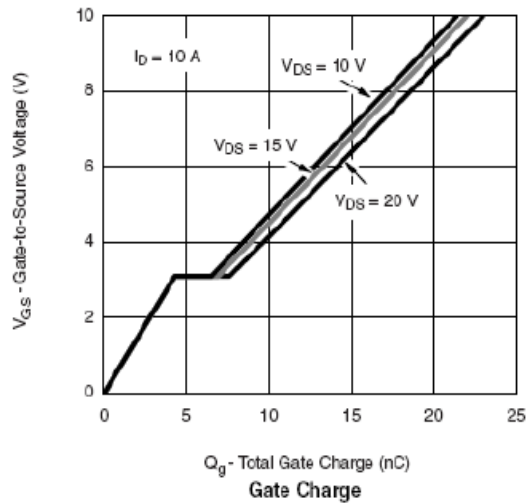


Dual N Channel Enhancement Mode MOSFET
8.5A

ELECTRICAL CHARACTERISTICS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\ \mu A$	1.0		3.0	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS} $T_J=55^{\circ}C$	$V_{DS}=24V_{GS}=0V$			1	
		$V_{DS}=24V_{GS}=0V$			5	uA
On-State Drain Current	$I_{D(on)}$	$V_{DS}\geq 5V, V_{GS}=10$	25			A
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=8.5A$ $V_{GS}=4.5V, I_D=7.8A$		0.012 0.015	0.014 0.018	Ω
Forward Tran Conductance	g_{fs}	$V_{DS}=15.0V, I_D=6.2A$		13		S
Diode Forward Voltage	V_{SD}	$I_S=2.3A, V_{GS}=0V$		0.8	1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=15V, V_{GS}=10V$ $I_D=2A$		16		nC
Gate-Source Charge	Q_{gs}			4.2		
Gate-Drain Charge	Q_{gd}			2.5		
Input Capacitance	C_{iss}	$V_{DS}=15.0V, V_{GS}=0V$ $f=1MHz$		1350		pF
Output Capacitance	C_{oss}			258		
Reverse TransferCapacitance	C_{rss}			150		
Turn-On Time	$t_{d(on)}^{tr}$	$V_{DD}=15V, R_L=15\ \Omega$ $I_D=5A, V_{GEN}=10V$ $R_G=1\ \Omega$		15	20	nS
				6	16	
Turn-Off Time	$t_{d(off)}^{tf}$			20	40	
				12	20	

TYPICAL CHARACTERISTICS (25°C Unless Note)


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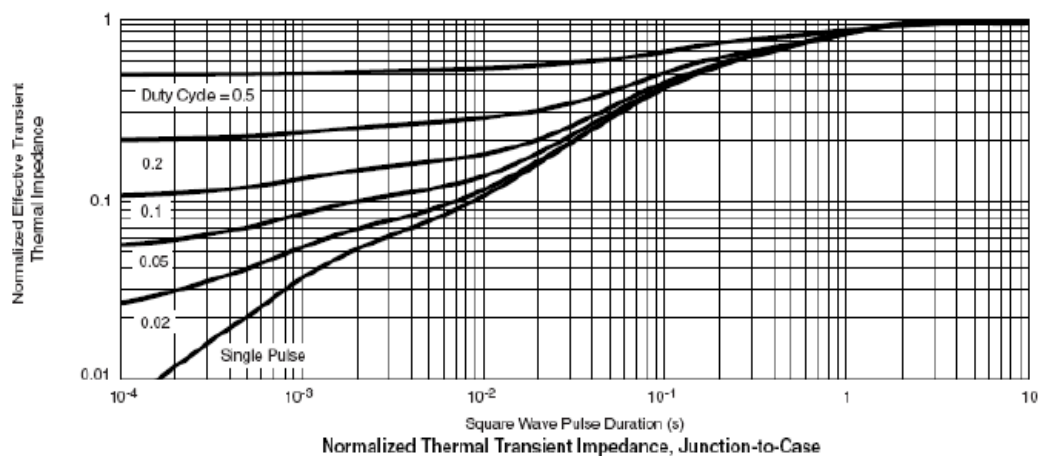
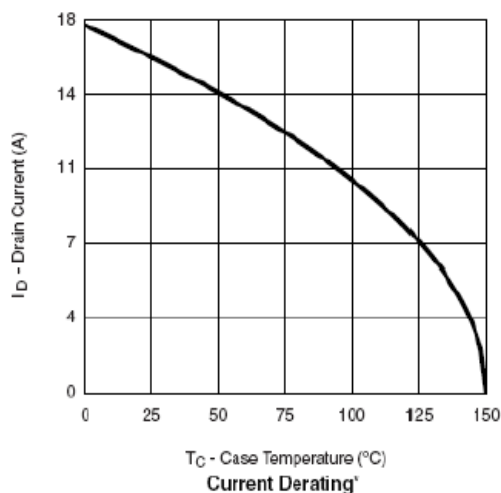
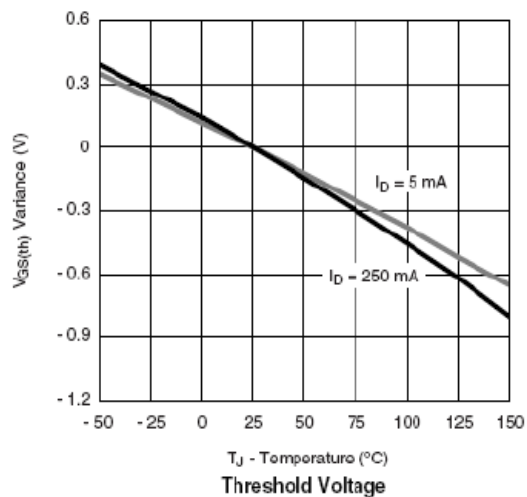


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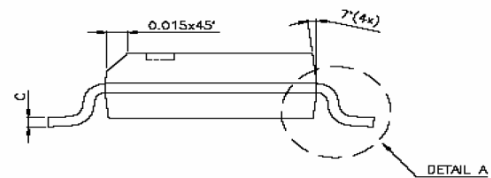
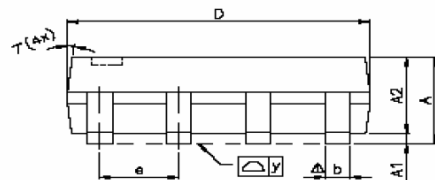
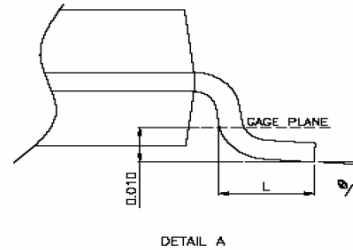
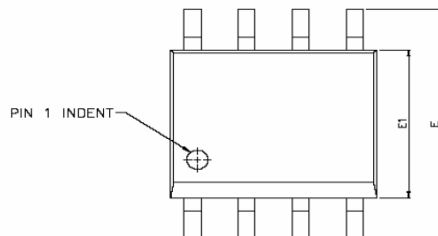
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SOP-8 PACKAGE OUTLINE


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	—	0.25	0.004	—	0.010
A2	—	1.45	—	—	0.057	—
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	—	1.27	—	—	0.050	—
L	0.38	0.71	1.27	0.015	0.028	0.050
Δy	—	—	0.076	—	—	0.003
θ	0°	—	8°	0°	—	8°