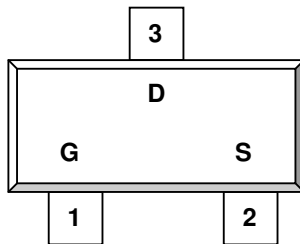


**DESCRIPTION**

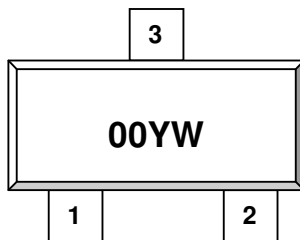
ST7400 is the N-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management, other battery powered circuits, and low in-line power loss are required. The product is in a very small outline surface mount package.

**PIN CONFIGURATION  
SOT-323 (SC-70)**


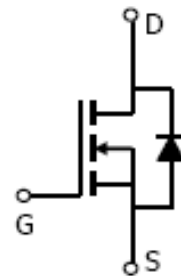
1.Gate 2.Source 3.Drain

**FEATURE**

- 30V/2.8A,  $R_{DS(ON)} = 77m\Omega$   
@ $V_{GS} = 10V$
- 30V/2.5A,  $R_{DS(ON)} = 85m\Omega$   
@ $V_{GS} = 4.5V$
- 30V/1.5A,  $R_{DS(ON)} = 170m\Omega$   
@ $V_{GS} = 2.5V$
- Super high density cell design for  
Extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and  
maximum DC current capability
- SOT-323 (SC-70) package design

**PART MARKING  
SOT-323**


Y: Year Code A: Process Code





**ST7400** 

N Channel Enhancement Mode MOSFET

2.8A

**ABSOLUTE MAXIMUM RATINGS** (Ta = 25°C Unless otherwise noted )

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V <sub>DSS</sub>	30	V
Gate-Source Voltage	V <sub>GSS</sub>	±12	V
Continuous Drain Current (T <sub>J</sub> =150°C)	I <sub>D</sub>	T <sub>A</sub> =25°C 2.8	A
		T <sub>A</sub> =70°C 2.3	
Pulsed Drain Current	I <sub>DM</sub>	10	A
Continuous Source Current (Diode Conduction)	I <sub>S</sub>	1.25	A
Power Dissipation	P <sub>D</sub>	T <sub>A</sub> =25°C 0.33	W
		T <sub>A</sub> =70°C 0.21	
Operation Junction Temperature	T <sub>J</sub>	150	°C
Storage Temperature Range	T <sub>STG</sub>	-55/150	°C
Thermal Resistance-Junction to Ambient	R <sub>θJA</sub>	100	°C/W



**ST7400** 

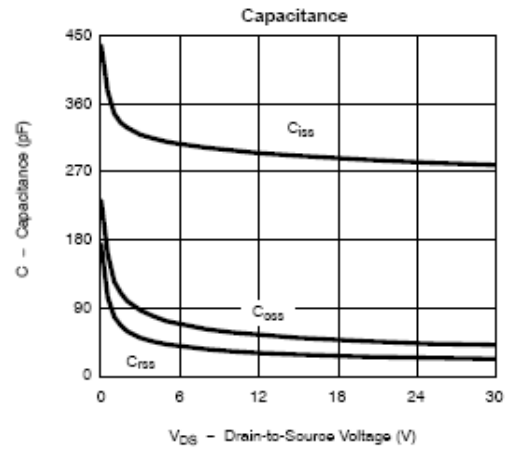
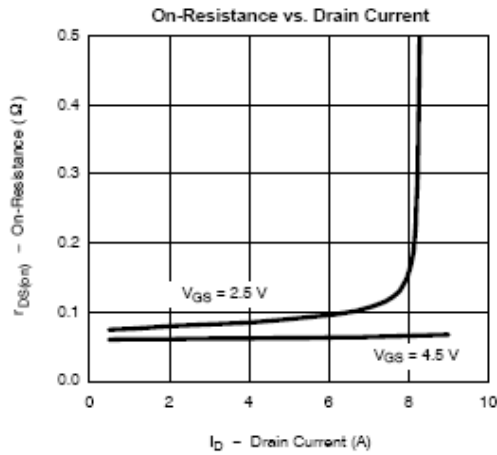
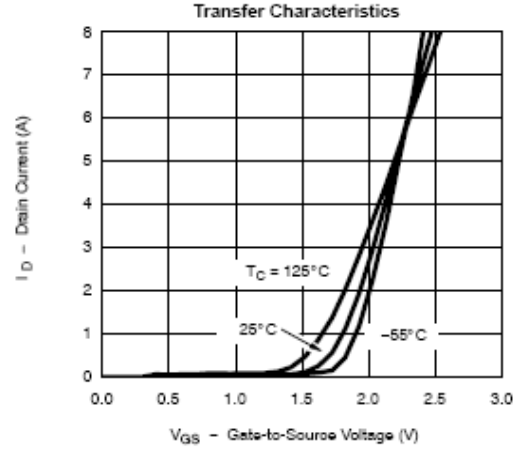
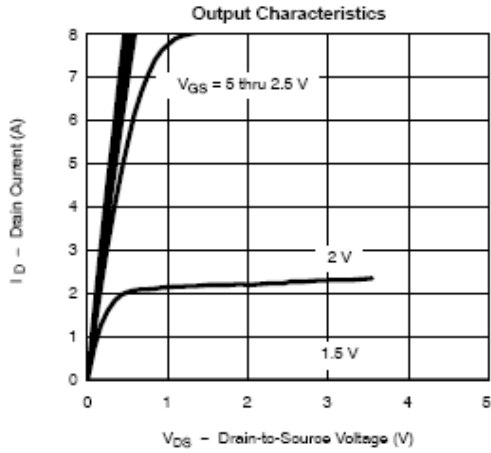
N Channel Enhancement Mode MOSFET

2.8A

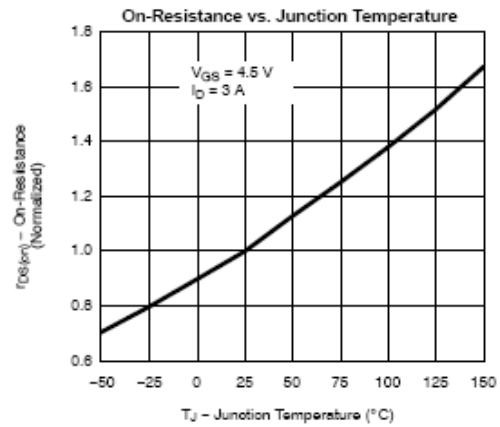
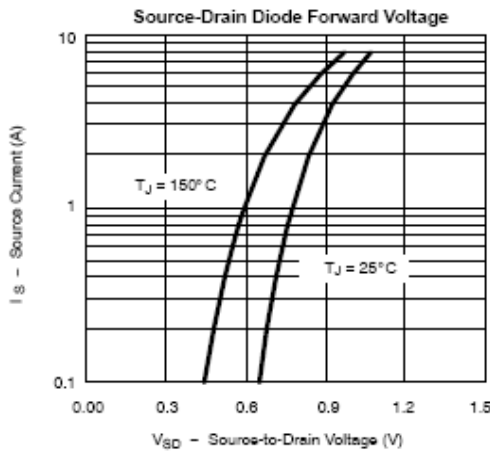
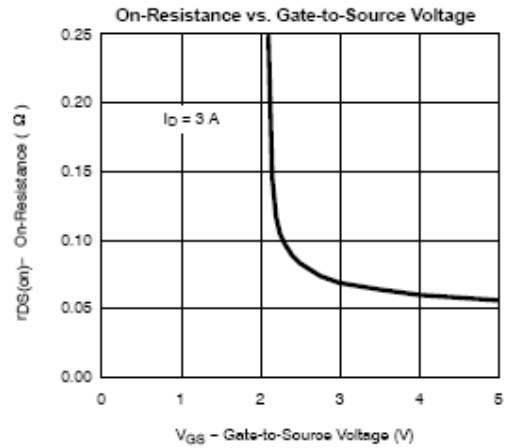
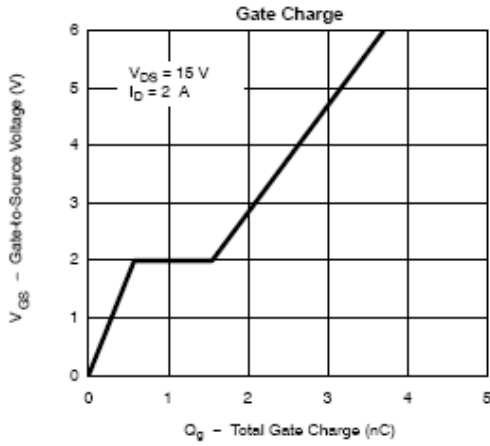
**ELECTRICAL CHARACTERISTICS** ( Ta = 25°C Unless otherwise noted )

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.8		1.6	V
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 12V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=24V, V_{GS}=0V$			1	uA
		$V_{DS}=24V, V_{GS}=0V$ $T_J=85^\circ C$			5	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \leq -5V, V_{GS}=-4.5V$	4.0			A
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=2.8A$		62	77	mΩ
		$V_{GS}=4.5V, I_D=2.3A$		70	85	
		$V_{GS}=2.5V, I_D=1.5A$		95	110	
Forward Transconductance	$g_{fs}$	$V_{DS}=5V, I_D=4.0V$		4		S
Diode Forward Voltage	$V_{SD}$	$I_S=1.0A, V_{GS}=0V$		0.8	1.2	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=15V$ $V_{GS}=4.5V$ $I_D=2.0A$		4.2		nC
Gate-Source Charge	$Q_{gs}$			0.6		
Gate-Drain Charge	$Q_{gd}$			1.5		
Input Capacitance	$C_{iss}$	$V_{DS}=15V$ $V_{GS}=0V$ $F=1MHz$		380		pF
Output Capacitance	$C_{oss}$			55		
Reverse Transfer Capacitance	$C_{rss}$			40		
Turn-On Time	$t_{d(on)}$ $t_r$	$V_{DS}=15V$ $I_D=1A$ $R_L=15\Omega$ $R_G=3\Omega$ $V_{GEN}=10V$		2.5		nS
Turn-Off Time	$t_{d(off)}$ $t_f$			2.5		
				20		
				5		

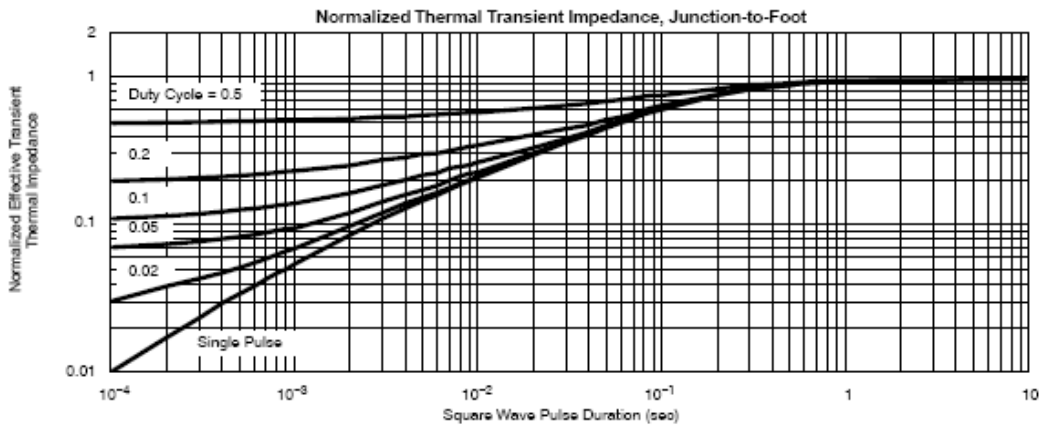
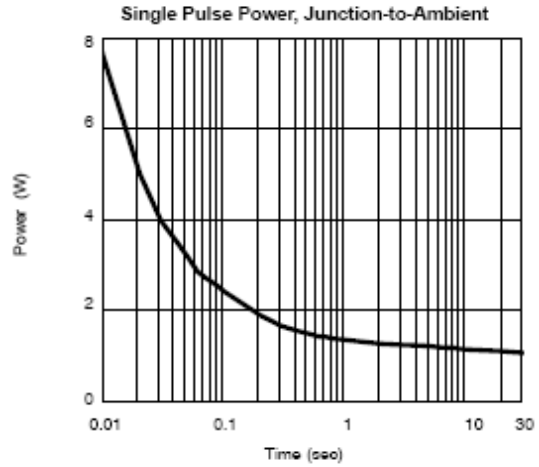
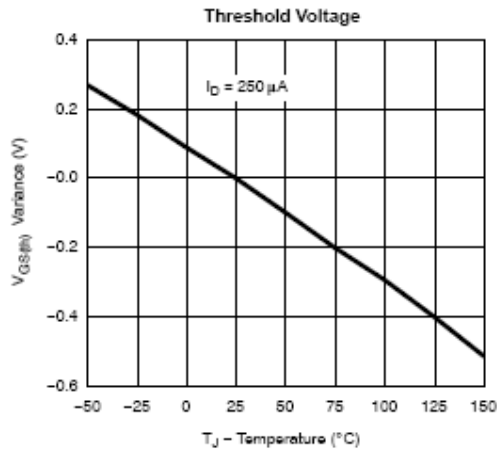
**TYPICAL CHARACTERISTICS**

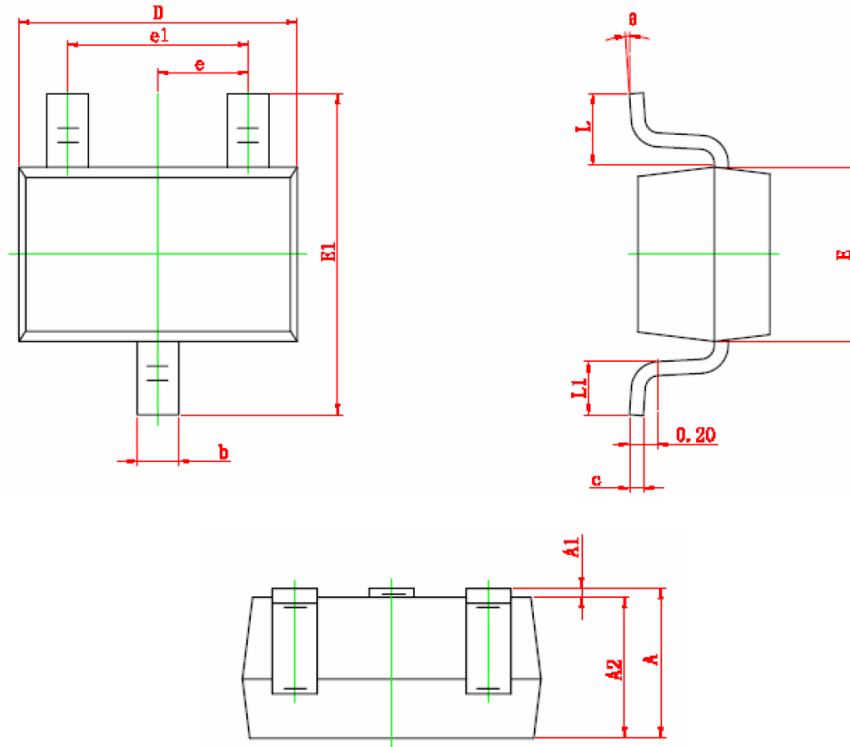


**TYPICAL CHARACTERISTICS**



**YPICAL CHARACTERICTICS**



**SOT-323 PACKAGE OUTLINE**


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.200	0.400	0.008	0.016
c	0.080	0.150	0.003	0.006
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650 TYP		0.026 TYP	
e1	1.200	1.400	0.047	0.055
L	0.525 REF		0.021 REF	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°



**ST7400**   
N Channel Enhancement Mode MOSFET

2.8A

---