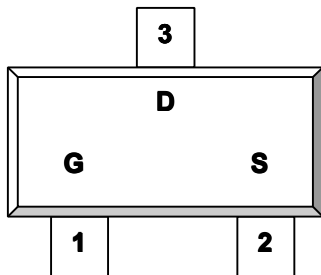


**DESCRIPTION**

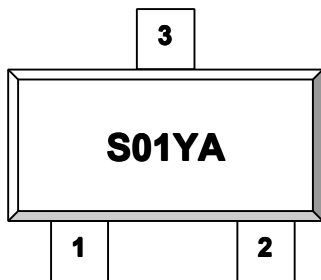
ST9401 is the P-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management, other battery powered circuits, and low in-line power loss are required. The product is in a very small outline surface mount package.

**PIN CONFIGURATION  
SOT-23**


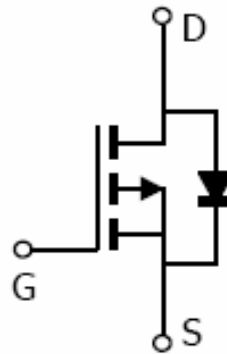
1. Gate 2. Source 3. Drain

**FEATURE**

- -20V/-2.8A,  $R_{DS(ON)} = 85m\Omega$   
@ $V_{GS} = -4.5V$
- -20V/-2.0A,  $R_{DS(ON)} = 120m\Omega$   
@ $V_{GS} = -2.5V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23 package design

**PART MARKING  
SOT-23**


Y: Year Code A: Process Code


**ORDERING INFORMATION**


Part Number	Package	Part Marking
ST9401SRG	SOT-23	S01YA

※ Process Code : A ~ Z ; a ~ z

※ ST9401SRG : S : SOT23 R : Tape Reel ; G : Pb - Free

STANSON TECHNOLOGY  
120 Bentley Square, Mountain View, Ca 94040 USA  
www.stansontech.com



**ST9401** 

P Channel Enhancement Mode MOSFET

**-3.0A**

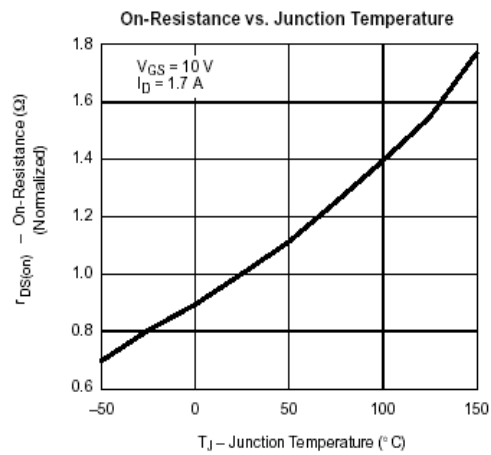
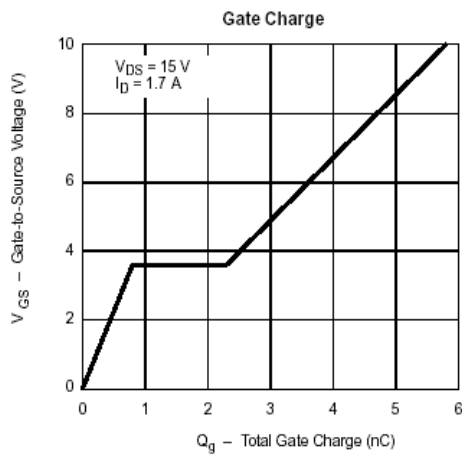
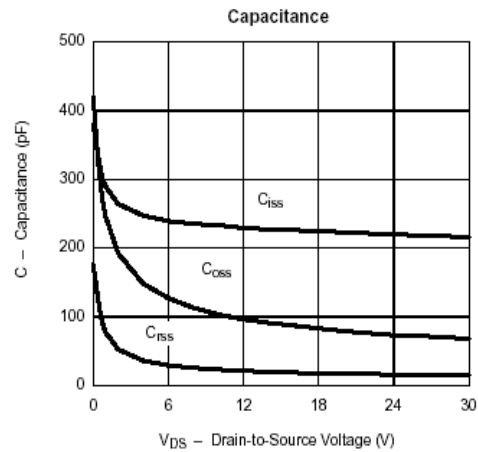
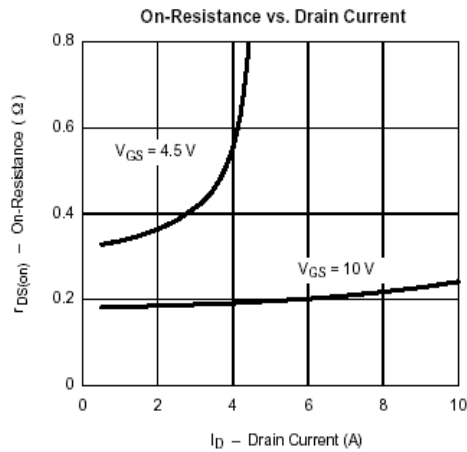
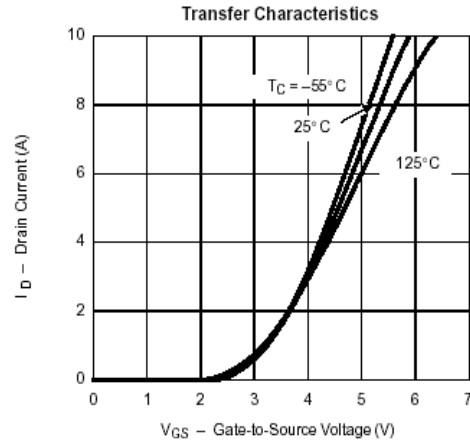
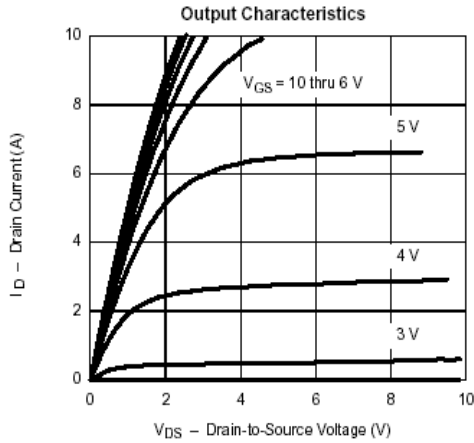
**ABSOLUTE MAXIMUM RATINGS** (Ta = 25°C Unless otherwise noted )

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V <sub>DSS</sub>	-20	V
Gate-Source Voltage	V <sub>GSS</sub>	±12	V
Continuous Drain Current (T <sub>J</sub> =150°C)	I <sub>D</sub>	T <sub>A</sub> =25°C -3.0	A
		T <sub>A</sub> =70°C -2.0	
Pulsed Drain Current	I <sub>DM</sub>	-10	A
Continuous Source Current (Diode Conduction)	I <sub>S</sub>	-1.6	A
Power Dissipation	P <sub>D</sub>	T <sub>A</sub> =25°C 1.25	W
		T <sub>A</sub> =70°C 0.8	
Operation Junction Temperature	T <sub>J</sub>	150	°C
Storage Temperature Range	T <sub>STG</sub>	-55/150	°C
Thermal Resistance-Junction to Ambient	R <sub>θJA</sub>	120	°C/W

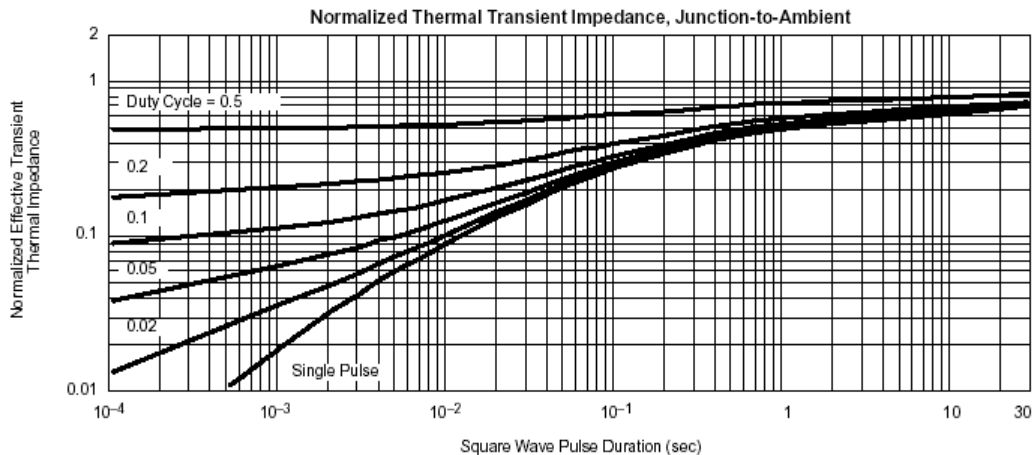
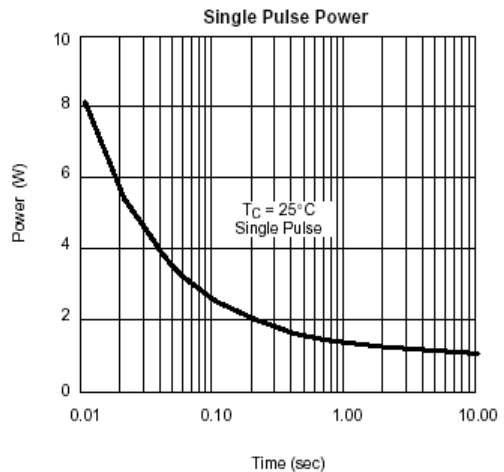
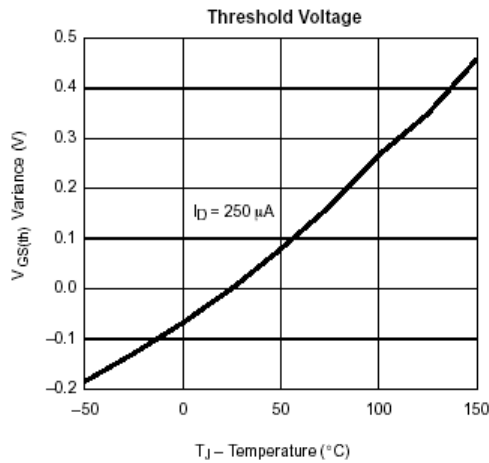
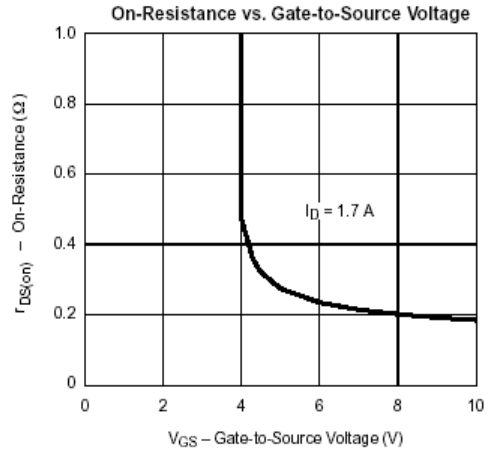
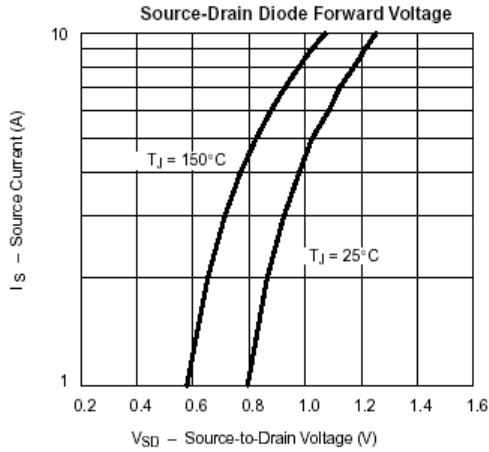
**ELECTRICAL CHARACTERISTICS** ( Ta = 25°C Unless otherwise noted )

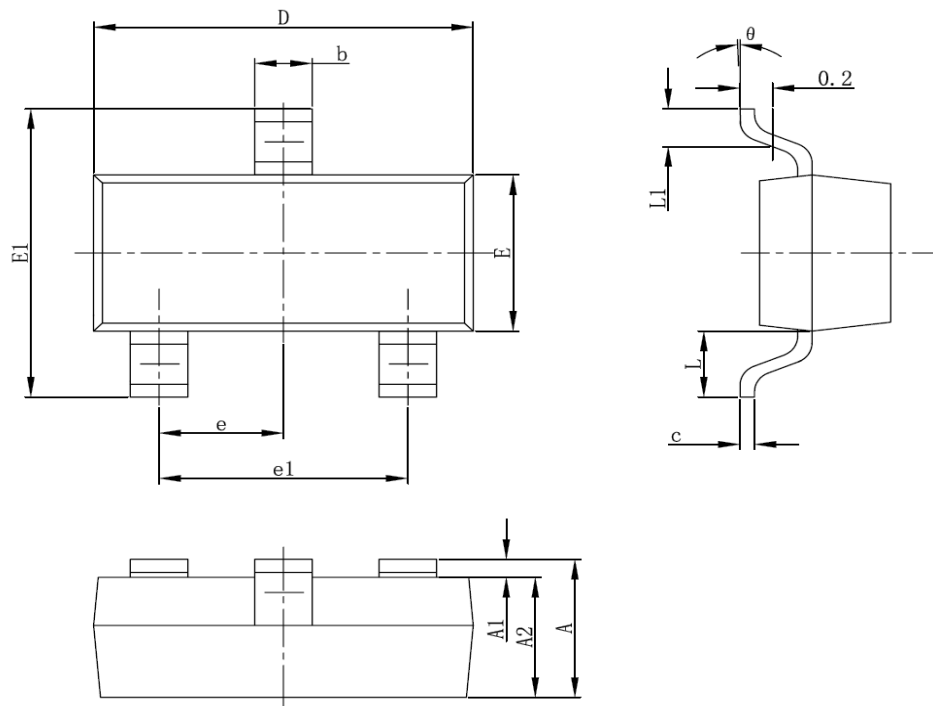
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-20			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.4		-1.	V
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 12V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-20V, V_{GS}=0V$			-1	uA
		$V_{DS}=-20V, V_{GS}=0V$ $T_J=55^\circ C$			-10	
On-State Drain Current	$I_{D(on)}$	$V_{DS}\leq -5V, V_{GS}=-4.5V$ $V_{DS}\leq -5V, V_{GS}=-2.5V$	-6 -3			A
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-2.8A$ $V_{GS}=-2.5V, I_D=-2.0A$		0.085 0.110	0.110 0.120	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS}=-5V, I_D=-2.8V$		6.5		S
Diode Forward Voltage	$V_{SD}$	$I_S=-1.6A, V_{GS}=0V$		-0.8	-1.2	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=-6V$ $V_{GS}=-4.5V$ $I_D=-2.8A$		5.8	10	nC
Gate-Source Charge	$Q_{gs}$			0.85		
Gate-Drain Charge	$Q_{gd}$			1.7		
Input Capacitance	$C_{iss}$	$V_{DS}=-6V$ $V_{GS}=0V$ $F=1MHz$		415		pF
Output Capacitance	$C_{oss}$			223		
Reverse Transfer Capacitance	$C_{rss}$			87		
Turn-On Time	$t_{d(on)}$ $t_r$	$V_{DD}=-6V$ $R_L=6\Omega$ $I_D=-1A$ $V_{GEN}=-4.5V$ $R_G=6\Omega$		13	25	nS
				36	60	
Turn-Off Time	$t_{d(off)}$ $t_f$			42	70	
				34	60	

**TYPICAL CHARACTERISTICS** (25°C Unless noted)



**TYPICAL CHARACTERISTICS** (25°C Unless noted)



**SOT-23 PACKAGE OUTLINE**


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.550REF		0.022REF	
L1	0.300	0.500	0.012	0.020
$\theta$	0°	8°	0°	8°