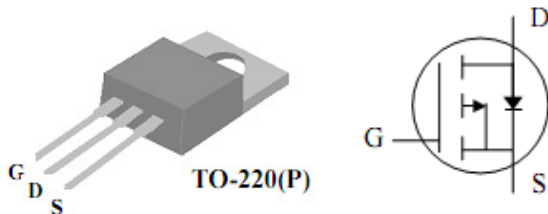




**DESCRIPTION**

ST9435GP is the P-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These device is particularly suited for low voltage application, notebook computer power management and other battery circuits where high-side switching.

**PIN CONFIGURATION**



**FEATURE**

- -30V/-10A,  $R_{DS(ON)} = 50m\Omega$   
@ $V_{GS} = -10V$
- -30V/-5A,  $R_{DS(ON)} = 80m\Omega$   
@ $V_{GS} = -4.5V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- TO-220 package design

**ABSOLUTE MAXIMUM RATINGS** ( $T_a = 25^\circ C$  Unless otherwise noted )

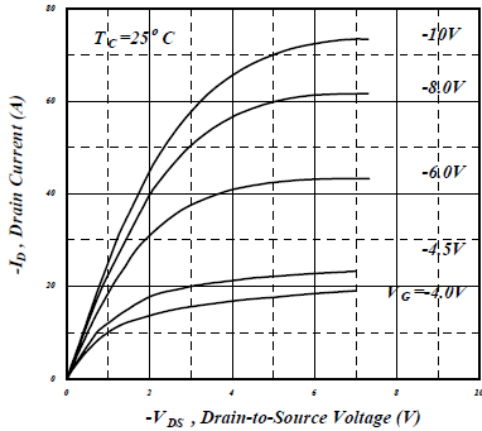
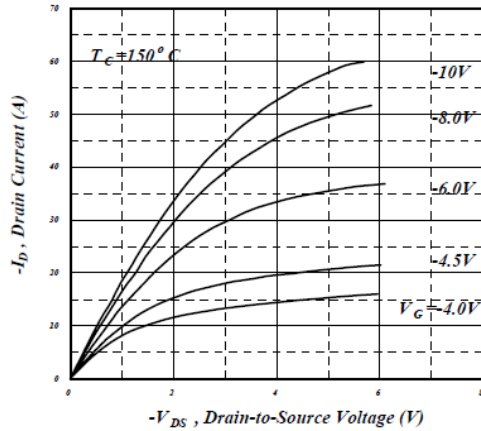
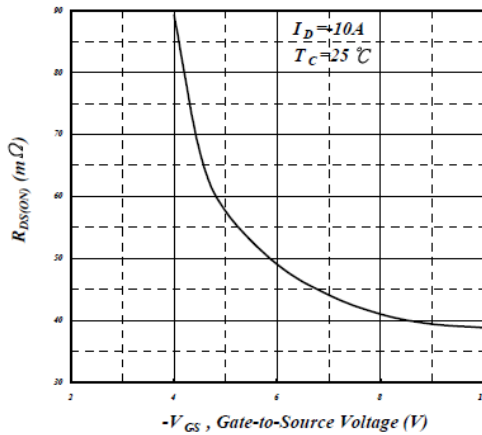
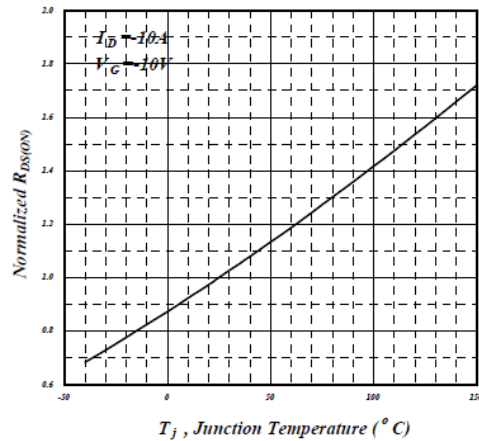
Parameter	Symbol	Typical	Unit
Drain-Source Voltage	VDSS	-30	V
Gate-Source Voltage	VGSS	±20	V
Continuous Drain Current ( $T_J = 150^\circ C$ )	ID	-15.0	A
		-8.0	
Pulsed Drain Current	IDM	-60	A
Power Dissipation	PD	62.5	W
Operation Junction Temperature	TJ	-55/150	°C
Storage Temperature Range	TSTG	-55/150	°C
Thermal Resistance-Junction to Ambient	RθJA	62	°C/W

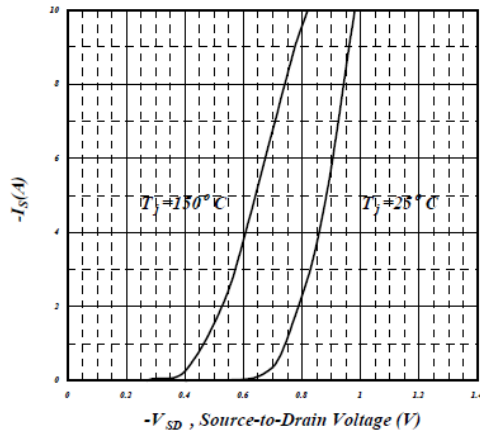
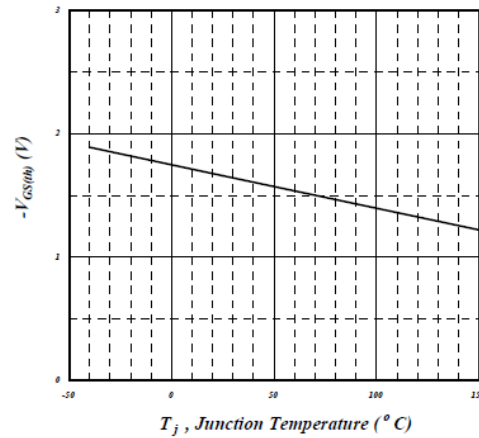
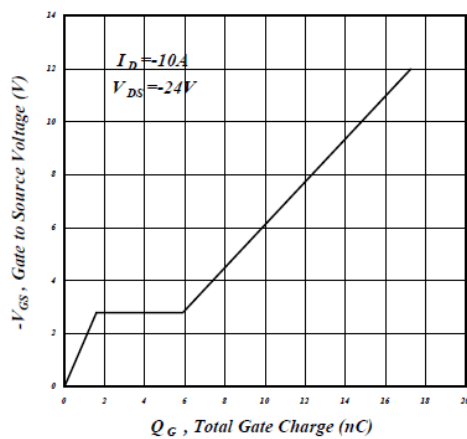
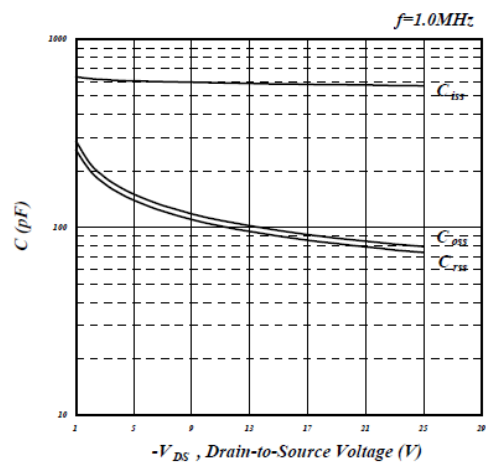


-15.0A

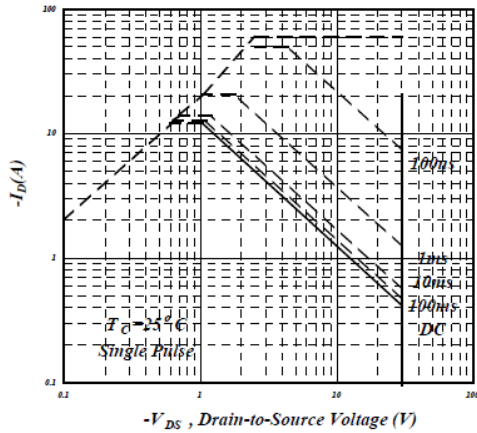
**ELECTRICAL CHARACTERISTICS** ( Ta = 25°C Unless otherwise noted )

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250mA$	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.0		-3.0	V
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-24V, V_{GS}=0V$			-1	uA
		$V_{DS}=-24V, V_{GS}=0V$ $T_J=125^\circ C$			-250	
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-10A$ $V_{GS}=-4.5V, I_D=-5A$		50 80	57 88	mΩ
Forward Transconductance	$g_{fs}$	$V_{DS}=-10V, I_D=-10A$		10		S
Diode Forward Voltage	$V_{SD}$	$I_S=-10A, V_{GS}=0V$			-1.2	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=-24V$ $V_{GS}=-4.5V$ $I_D=-10A$		9	16	nC
Gate-Source Charge	$Q_{gs}$			1.6		
Gate-Drain Charge	$Q_{gd}$			4.3		
Input Capacitance	$C_{iss}$	$V_{DS}=-25V$ $V_{GS}=0V$ $F=1MHz$		575	750	pF
Output Capacitance	$C_{oss}$			80		
Reverse Transfer Capacitance	$C_{rss}$			75		
Turn-On Time	$t_{d(on)}$	$V_{DS}=-15V, R_G=3.3\Omega$ $I_D=-10A, V_{GS}=-10V$ $R_D=1.5\Omega$		6.8		nS
	$t_r$			46		
Turn-Off Time	$t_{d(off)}$			20		
	$t_f$			7		

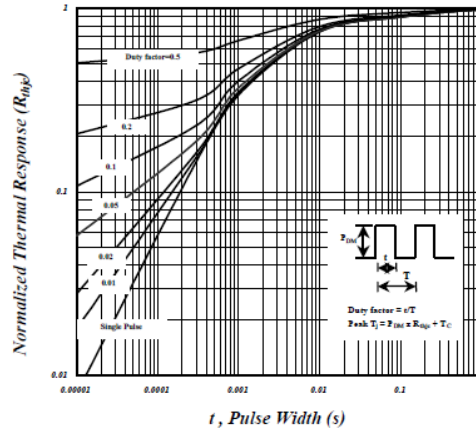
**TYPICAL CHARACTERISTICS**

**Fig 1. Typical Output Characteristics**

**Fig 2. Typical Output Characteristics**

**Fig 3. On-Resistance v.s. Gate Voltage**

**Fig 4. Normalized On-Resistance v.s. Junction Temperature**

**TYPICAL CHARACTERISTICS**

**Fig 5. Forward Characteristic of Reverse Diode**

**Fig 6. Gate Threshold Voltage v.s. Junction Temperature**

**Fig 7. Gate Charge Characteristics**

**Fig 8. Typical Capacitance Characteristics**

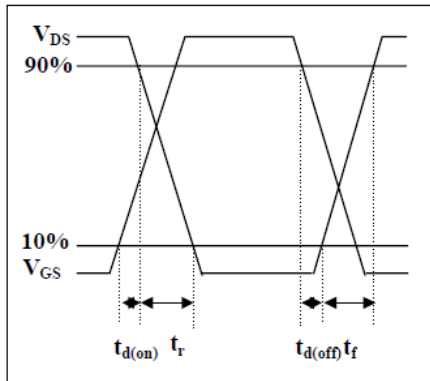
**TYPICAL CHARACTERISTICS**



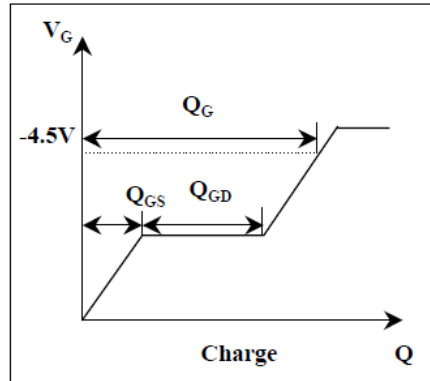
**Fig 9. Maximum Safe Operating Area**



**Fig 10. Effective Transient Thermal Impedance**

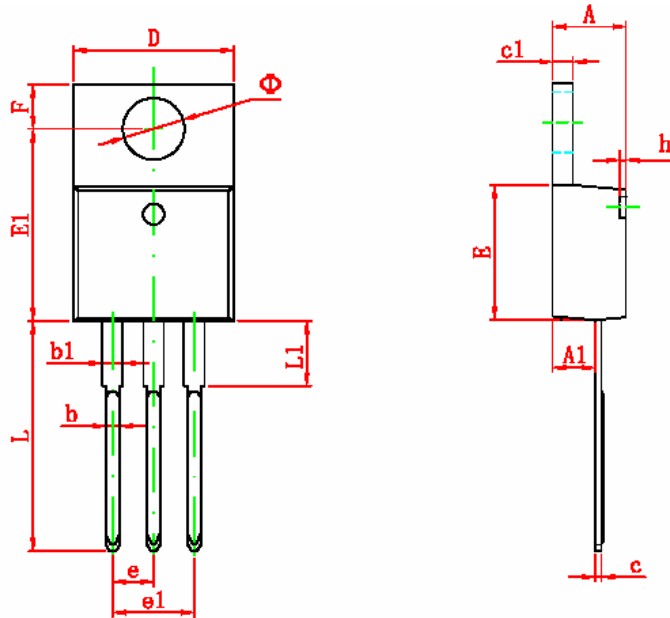


**Fig 11. Switching Time Waveform**



**Fig 12. Gate Charge Waveform**

**TO-220-3L PACKAGE OUTLINE**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.470	4.670	0.176	0.184
A1	2.520	2.820	0.099	0.111
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.310	0.530	0.012	0.021
c1	1.170	1.370	0.046	0.054
D	10.010	10.310	0.394	0.406
E	8.500	8.900	0.335	0.350
E1	12.060	12.460	0.475	0.491
e	2.540 TYP		0.100 TYP	
e1	4.980	5.180	0.196	0.204
F	2.590	2.890	0.102	0.114
h	0.000	0.300	0.000	0.012
L	13.400	13.800	0.528	0.543
L1	3.560	3.960	0.140	0.156
• •	3.735	3.935	0.147	0.155