STC6614

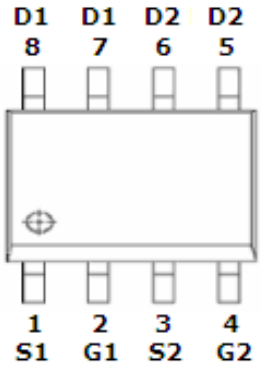
N&P Pair Enhancement Mode MOSFET

7.0A / -5.0A

DESCRIPTION

The STC6614 is the N & P-Channel enhancement mode power field effect transistor using high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance and provide superior switching performance. This device is particularly suited for low voltage application such as notebook computer power management and other battery powered circuits, where high-side switching, low in-line power loss and resistance to transient are needed.

PIN CONFIGURATION
SOP-8



PART MARKING

Y：Year
A：Product Code
Q：Process Code

FEATURE

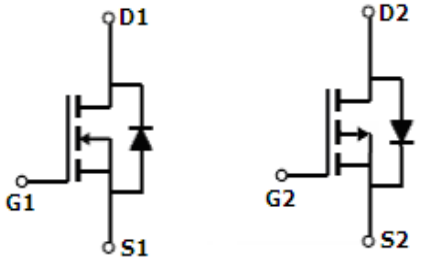
N-Channel

- 60V/7.0A, $R_{DS(ON)}$ = 35mΩ(Typ.) @V_{GS} = 10V
- 60V/4.0A, $R_{DS(ON)}$ = 40mΩ @V_{GS} = 4.5V

P-Channel

- -60V/-5.0A, $R_{DS(ON)}$ = 60mΩ(Typ.) @V_{GS} = -10V
- -60V/-3.0A, $R_{DS(ON)}$= 80mΩ @V_{GS} = -4.5V

- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOP-8 package



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ABSOULTE MAXIMUM RATINGS (Ta = 25℃ Unless otherwise noted)

Parameter		Symbol	Typical N	Typical P	Unit
Drain-Source Voltage		V_{DSS}	60	-60	V
Gate-Source Voltage		V_{GSS}	±20	±20	V
Continuous Drain Current (TJ=150℃)	T_A=25℃ T_A=70℃	I_D	7.0 5.2	-5.0 -4.0	A
Pulsed Drain Current		I_{DM}	40	-30	A
Continuous Source Current (Diode Conduction)		I_S	3	-3	A
Power Dissipation	T_A=25℃ T_A=70℃	P_D	2.3 1.3	2.3 1.3	W
Operation Junction Temperature		T_J	150		℃
Storgae Temperature Range		T_{STG}	-55/150		℃
Thermal Resistance-Junction to Ambient	T≦10Sec Sready State	$R_{\theta JA}$	62.5 110	62.5 110	℃/W

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ELECTRICAL CHARACTERISTICS (Ta = 25℃ Unless otherwise noted)

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Static							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA V_{GS}=0V,I_D=-250uA	N P	60 -60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=VGS,I_D=250 uA V_{DS}=VGS,I_D=-250uA	N P	1.0 -1.0		3.0 -3.0	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V V_{DS}=0V,V_{GS}=±20V	N P			±100 ±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=48V,V_{GS}=0V V_{DS}=-48V,V_{GS}=0V	N P			1 -1	uA
	T_J=55℃	V_{DS}=48V,V_{GS}=0V V_{DS}=-48V,V_{GS}=0V	N P			5 -5	
On-State Drain Current	$I_{D(on)}$	V_{DS}≧5V,V_{GS}=10V V_{DS}≦-5V,V_{GS}=-10V	N P	20 -20			A
Drain-source On-Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=10.0A V_{GS}=-10V,I_D=-10.0A	N P		0.035 0.060	0.040 0.072	Ω
		V_{GS}=4.5V, I_D=6.0A V_{GS}=-4.5V,I_D=-5.0 A	N P		0.040 0.080	0.048 0.093	
Forward Tran Conductance	gfs	V_{DS}=5V,I_D=6.3A V_{DS}=-5V,I_D=-5.9A	N P		27 18		S
Diode Forward Voltage	V_{SD}	I_S=1.0A,V_{GS}=0V I_S=-1.7A,V_{GS}=0V	N P			1.2 -1.2	V
Dynamic							
Total Gate Charge	Q_g	**N-Channel** V_{DS}=30V,V_{GS}=10V	N P		47.7 45.2		nC
Gate-Source Charge	Q_{gs}	I_D≡6.3A **P-Channel**	N P		6 5.8		
Gate-Drain Charge	Q_{gd}	V_{DS}=-30V,V_{GS}=-10V I_D≡-5.0A	N P		14.5 9.6		
Turn-On Time	$t_{d(on)}$ t_r	**N-Channel** V_{DS}=30V,R_L=4.7Ω	N P		8 9		nS
		V_{GS}=10V,R_{GEN}=3Ω	N P		9 6.2		
Turn-Off Time	$t_{d(off)}$ t_f	**P-Channel** V_{DS}=-30V,R_L=6.2Ω	N P		25 44		
		V_{GS}=-10V,R_{GEN}=3Ω	N P		10 13.2		

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TYPICAL CHARACTERICTICS (N MOS)

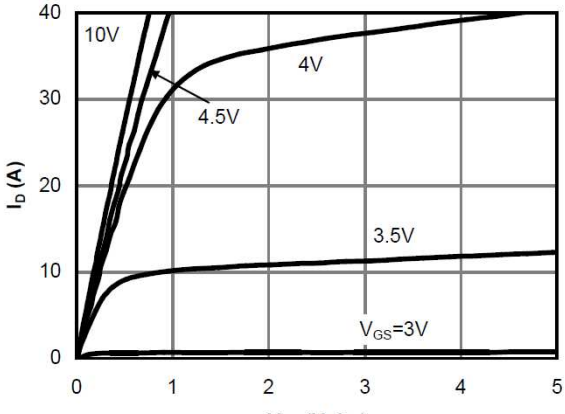

Fig 1: On-Region Characteristics

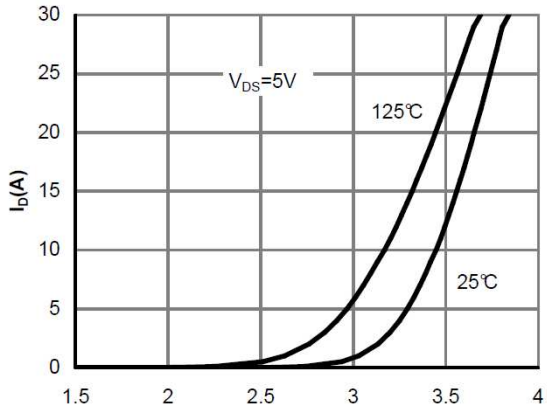

Figure 2: Transfer Characteristics

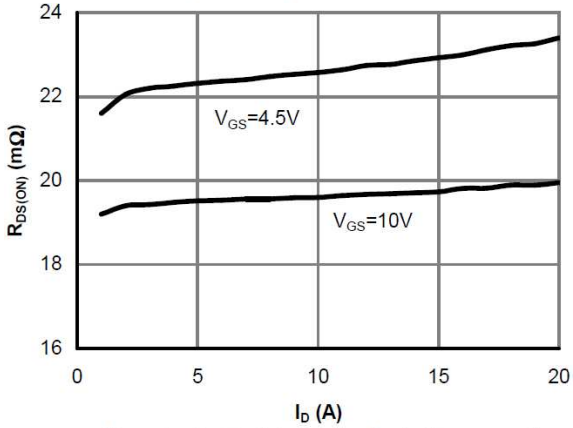

Figure 3: On-Resistance vs. Drain Current and Gate Voltage

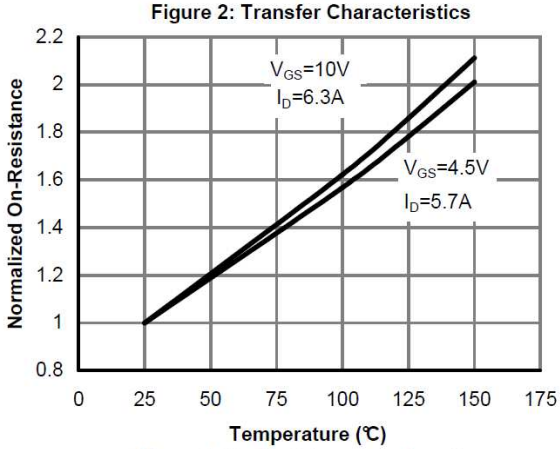

Figure 4: On-Resistance vs. Junction Temperature

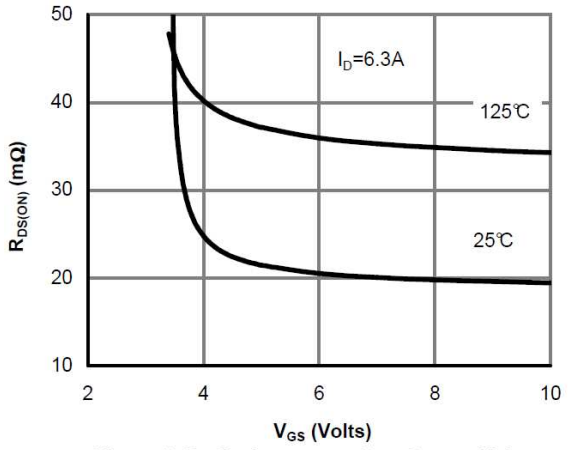

Figure 5: On-Resistance vs. Gate-Source Voltage

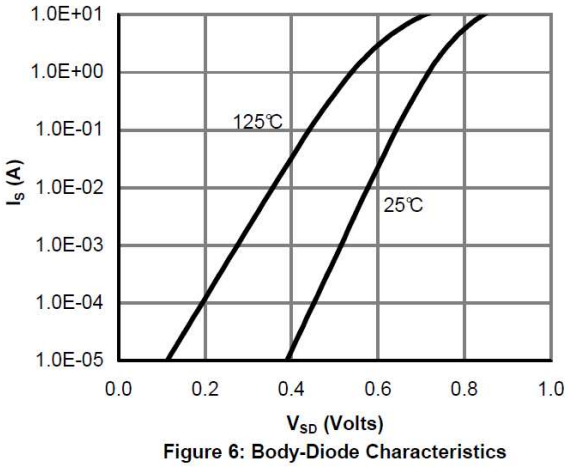

Figure 6: Body-Diode Characteristics

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TYPICAL CHARACTERICTICS (N MOS)

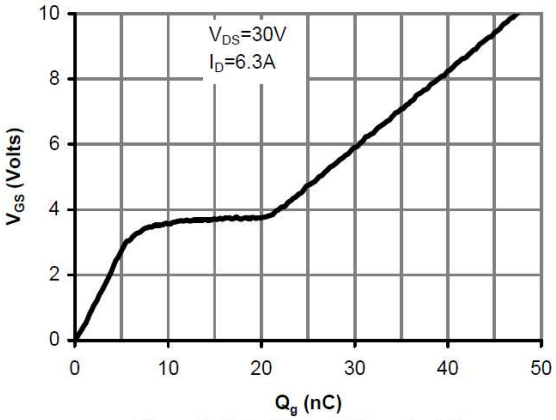

Figure 7: Gate-Charge Characteristics

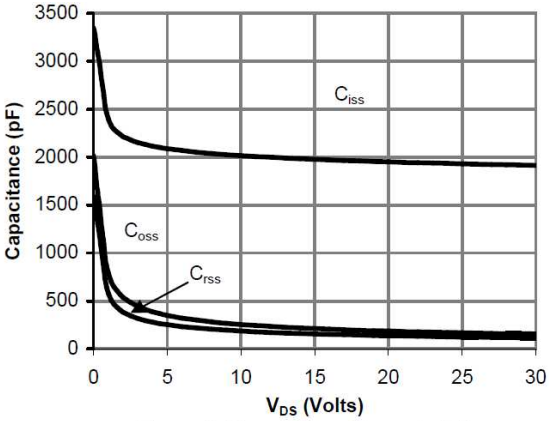

Figure 8: Capacitance Characteristics

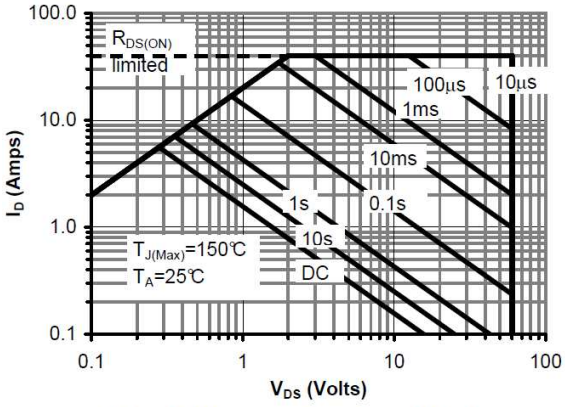

Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

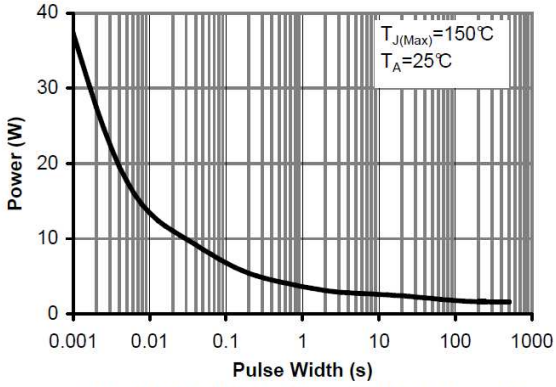

Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

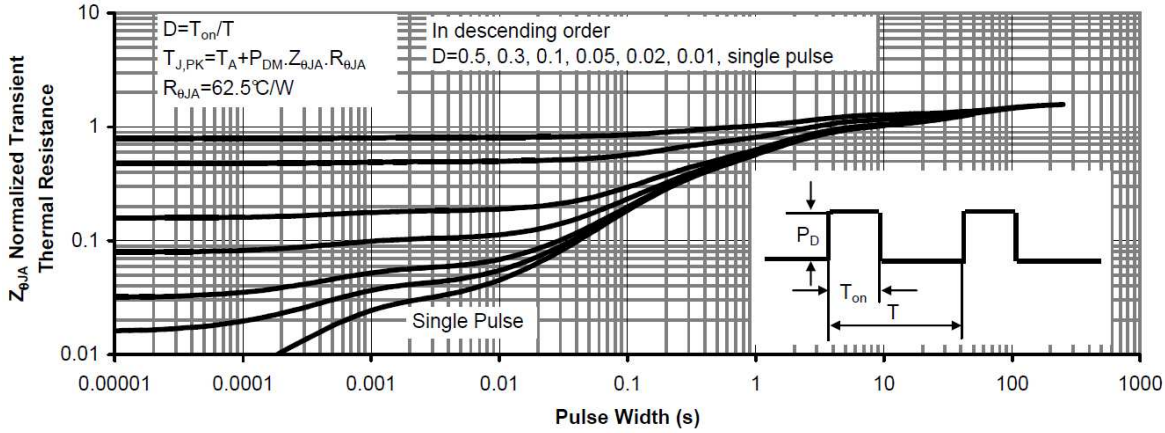

Figure 11: Normalized Maximum Transient Thermal Impedance

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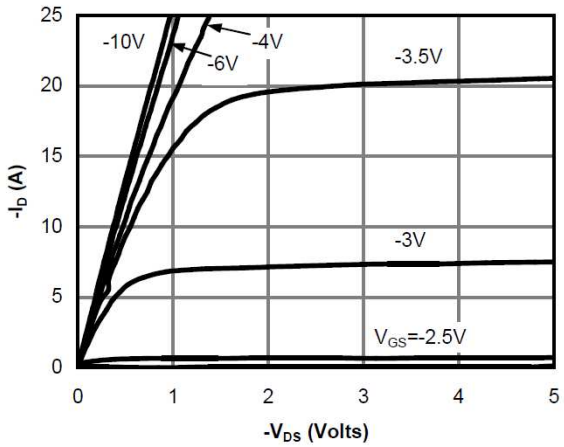
YPICAL CHARACTERICTICS (P MOS)



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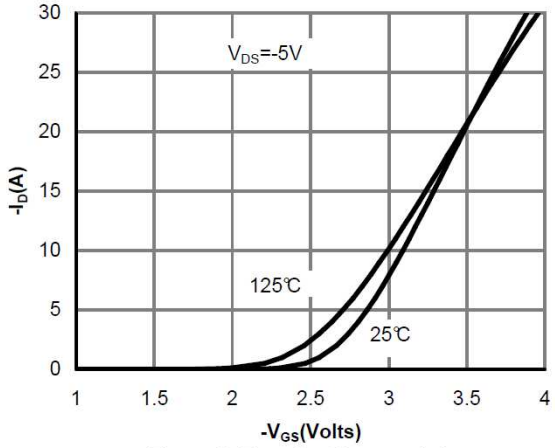


Figure 2: Transfer Characteristics

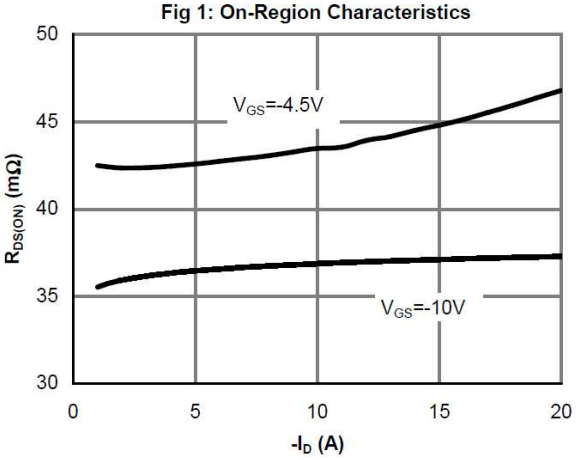


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

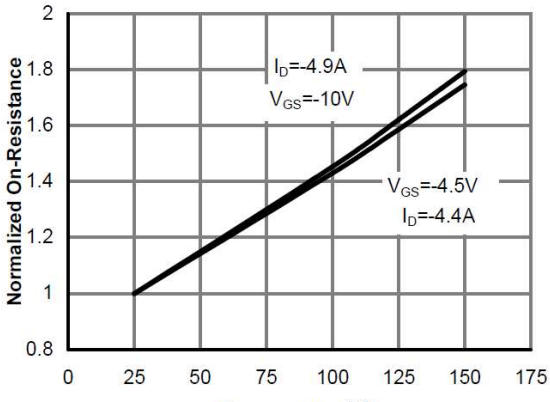


Figure 4: On-Resistance vs. Junction Temperature

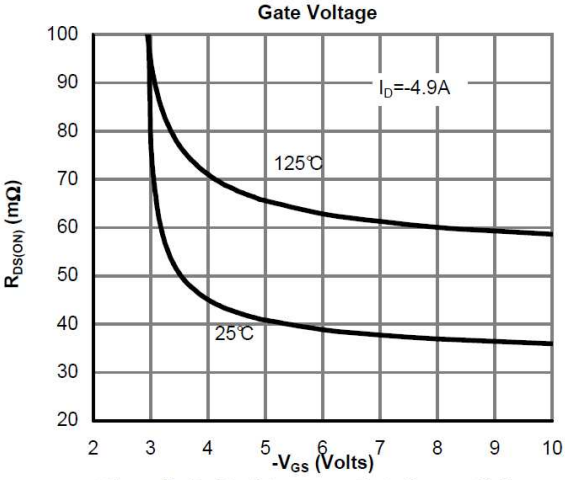
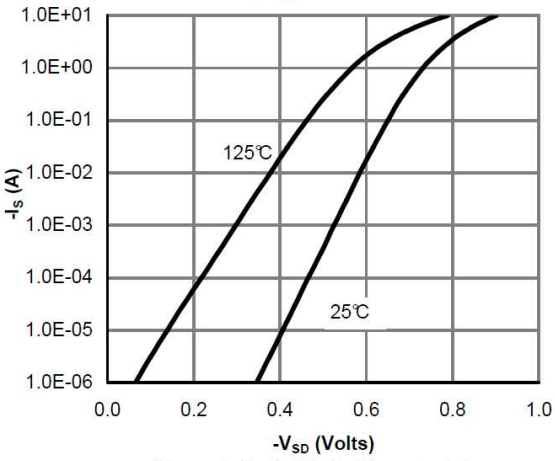


Figure 5: On-Resistance vs. Gate-Source Voltage



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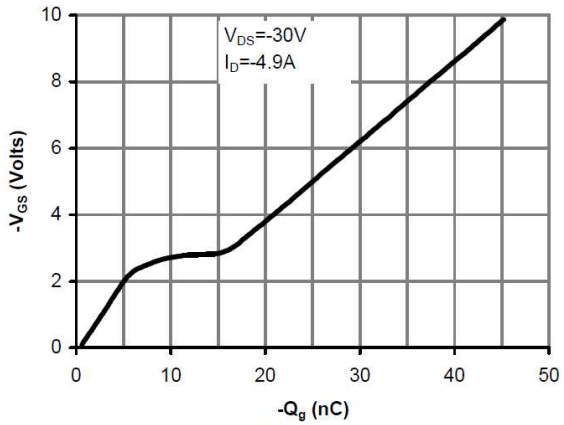
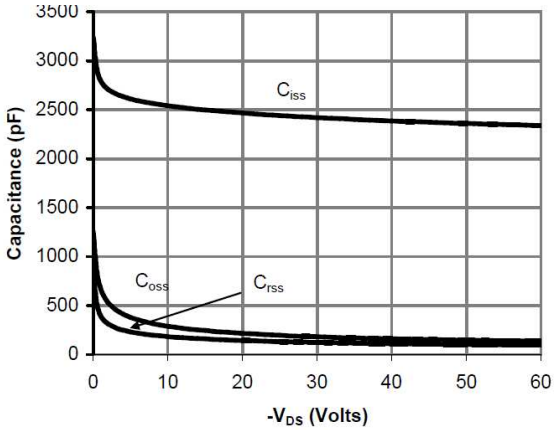


Figure 7: Gate-Charge Characteristics



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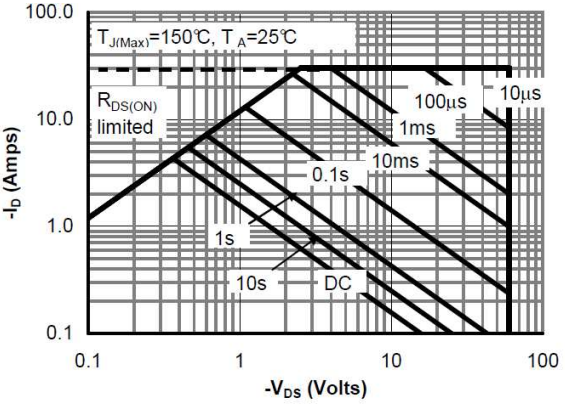

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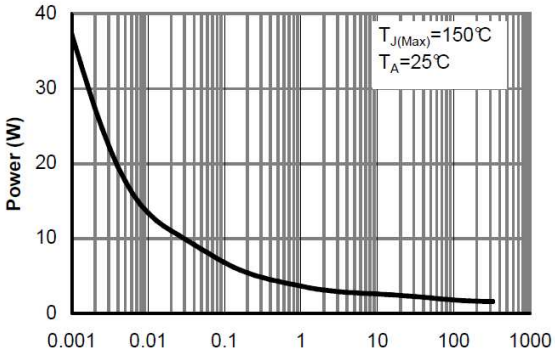

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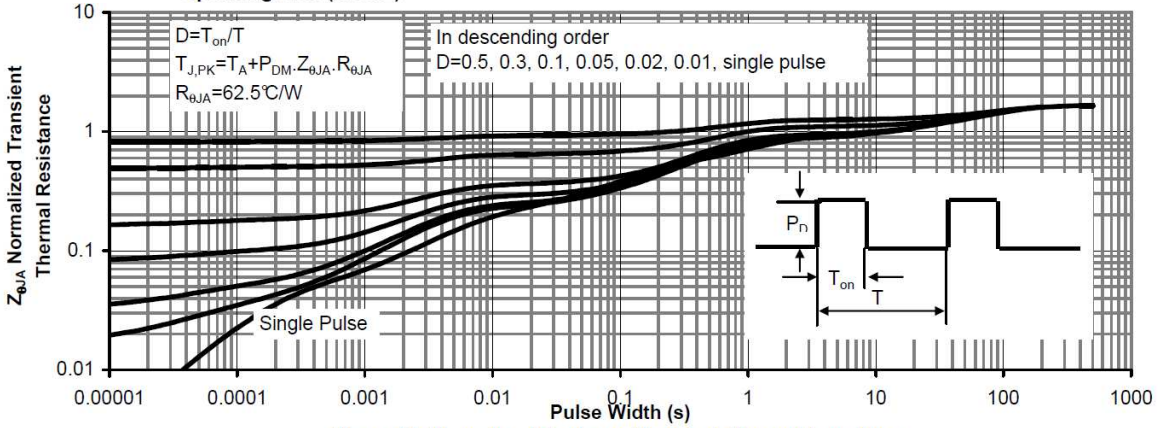
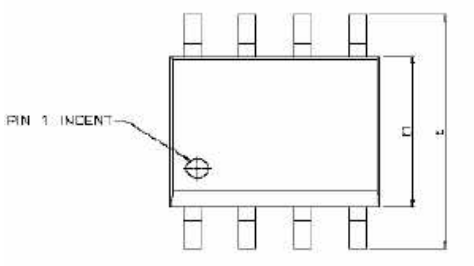
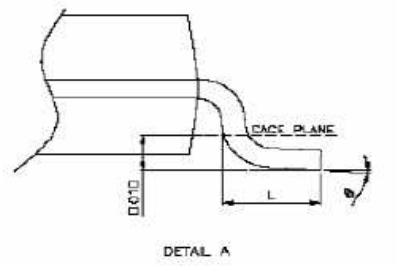
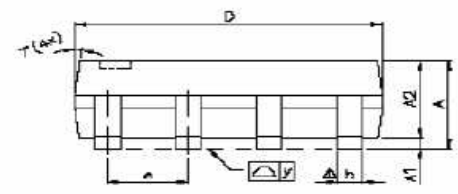


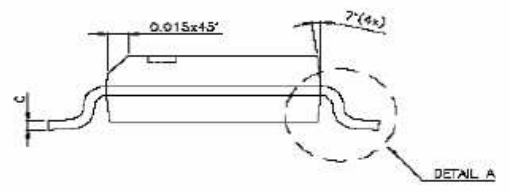
Figure 11: Normalized Maximum Transient Thermal Impedance

SOP-8 PACKAGE OUTLINE









SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	——	0.25	0.004	——	0.010
A2	——	1.45	——	——	0.057	——
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	——	1.27	——	——	0.050	——
L	0.38	0.71	1.27	0.015	0.028	0.050
⚠2 y	——	——	0.076	——	——	0.003
θ	0°	——	8°	0°	——	8°

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