STANSON

STN4186D

N Channel Enhancement Mode MOSFET

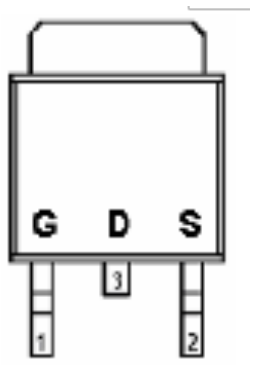
35.0A

DESCRIPTION

STN4186D is the N-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. The STN454D has been designed specially to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

PIN CONFIGURATION (D-PAK)

TO-252

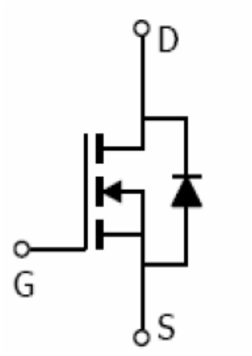


FEATURE

- 40V/20.0A, $R_{DS(ON)}$ = 13mΩ (Typ.) @V_{GS} = 10V
- 40V/15.0A, $R_{DS(ON)}$ = 15mΩ @V_{GS} = 4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- TO-252 package design

PART MARKING

Y: Year Code
A: Date Code
B: Wafer Code



ABSOULTE MAXIMUM RATINGS (Ta = 25℃ Unless otherwise noted)

Parameter		**Symbol**	**Typical**	**Unit**
Drain-Source Voltage		VDSS	40	V
Gate-Source Voltage		VGSS	±20	V
Pulsed Drain Current		IDM	70	A
Continuous Source Current (Diode Conduction)		IS	35	A
Power Dissipation	TA=25℃	PD	50	W
	TA=70℃		25	
Operation Junction Temperature		TJ	150	℃
Storgae Temperature Range		TSTG	-55/150	℃
Thermal Resistance-Junction to Ambient		RθJA	60	℃/W

ELECTRICAL CHARACTERISTICS (Ta = 25℃ Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,ID=250uA	40			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},ID=250uA	1.0		2.5	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40V,V_{GS}=0V			1	uA
		V_{DS}=40V,V_{GS}=0V T_J=85℃			5	
Drain-source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=20A V_{GS}=4.5V,I_D=15A		13 15	15 19	mΩ
Forward Transconductance	gfs	V_{DS}=5V,I_D=12A		60		S
Diode Forward Voltage	V_{SD}	I_S=3.0A,V_{GS}=0V			1.1	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=10V,V_{DS}=20 I_D=20A		18		nC
Gate-Source Charge	Q_{gs}			10		
Gate-Drain Charge	Q_{gd}			5		
Input Capacitance	C_{iss}	V_{DS} =20V,VGS=0V F=1MHz		1000		pF
Output Capacitance	C_{oss}			130		
Reverse TransferCapacitance	C_{rss}			85		
Turn-On Time	$t_{d(on)}$	V_{DD}=20V,R_L= 4Ω I_D=5.0A,V_{GEN}=10V R_G=1Ω		6	12	nS
	tr			13	20	
Turn-Off Time	$t_{d(off)}$			26	36	
	tf			7.5	12	

TYPICAL CHARACTERICTICS

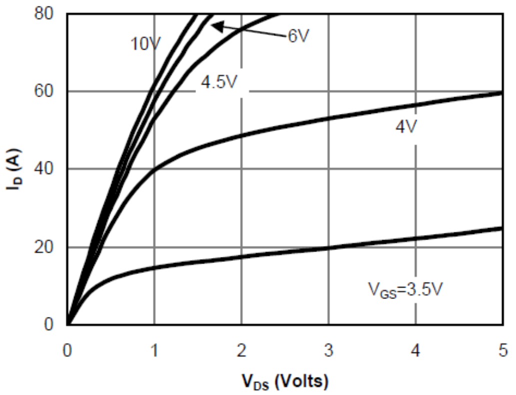


Fig 1: On-Region Characteristics (Note E)

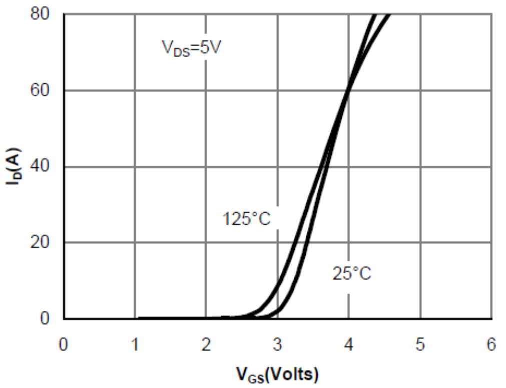


Figure 2: Transfer Characteristics (Note E)

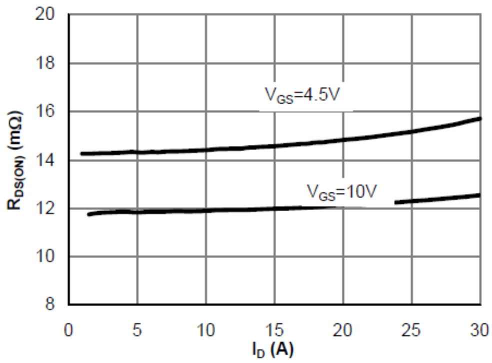


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

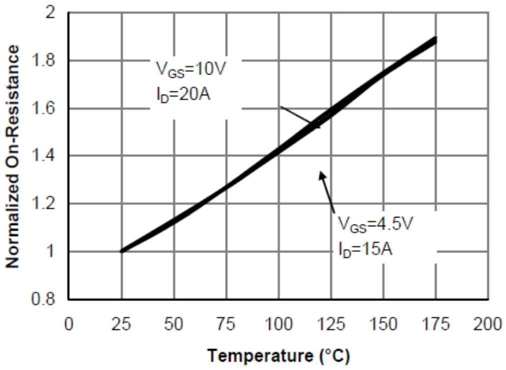


Figure 4: On-Resistance vs. Junction Temperature (Note E)

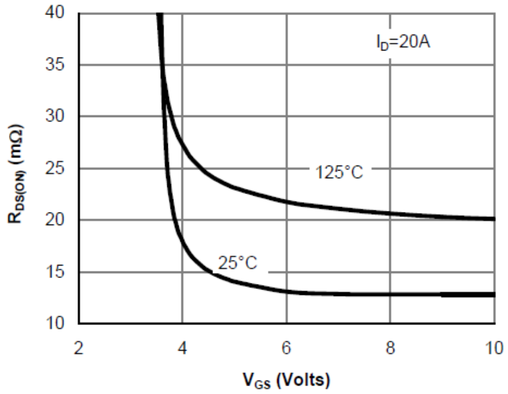


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

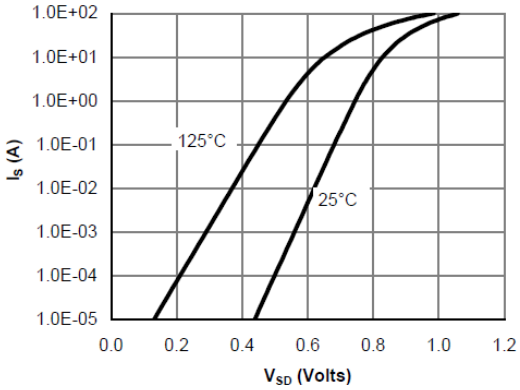


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL CHARACTERICTICS

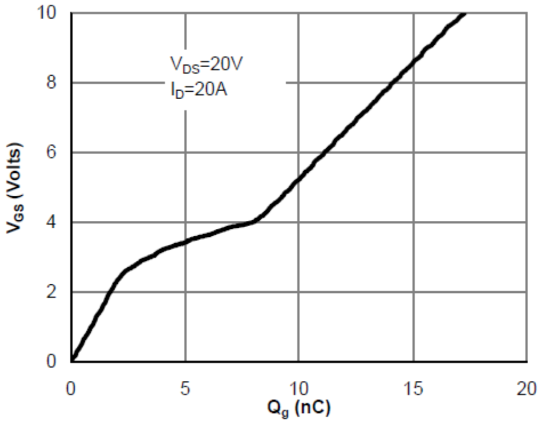


Figure 7: Gate-Charge Characteristics

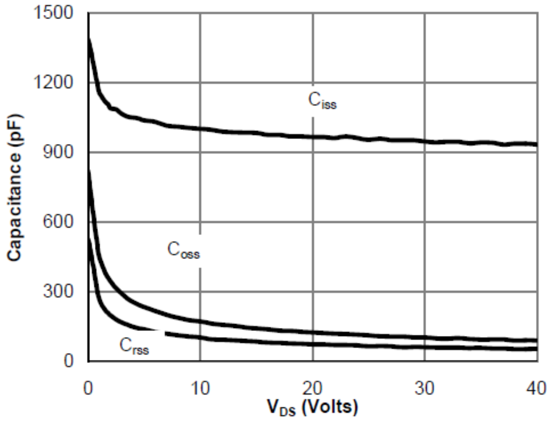


Figure 8: Capacitance Characteristics

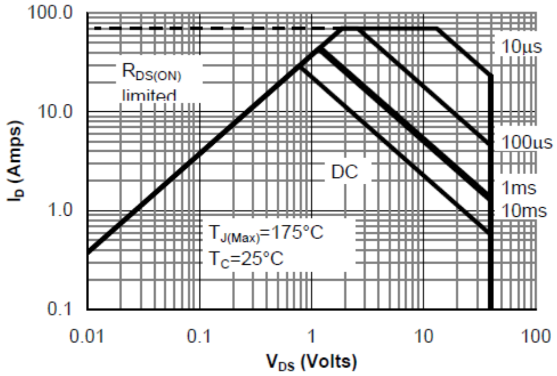


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

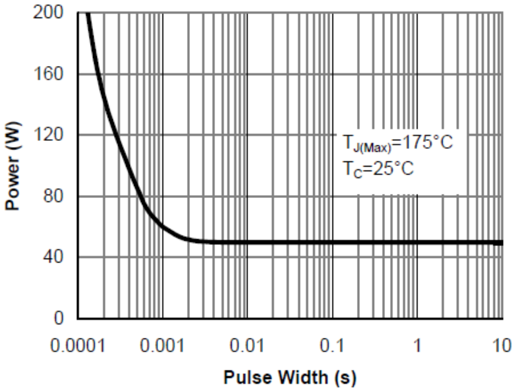


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

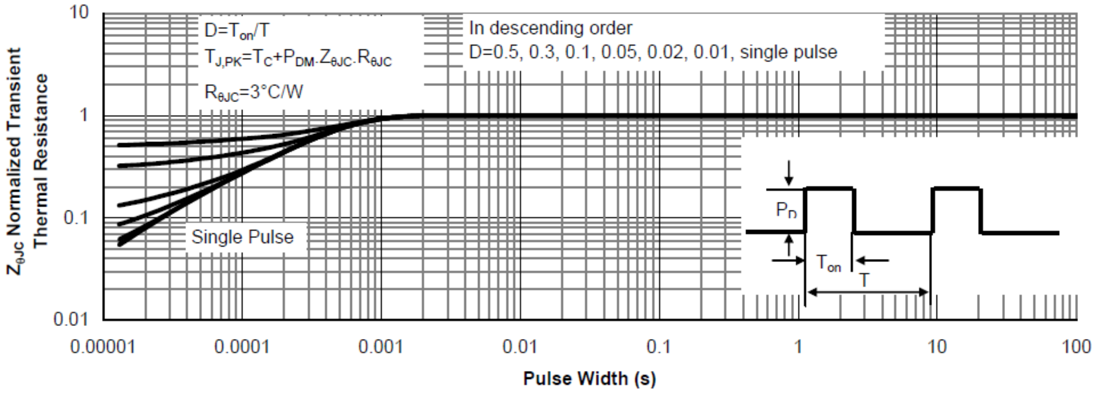


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL CHARACTERICTICS

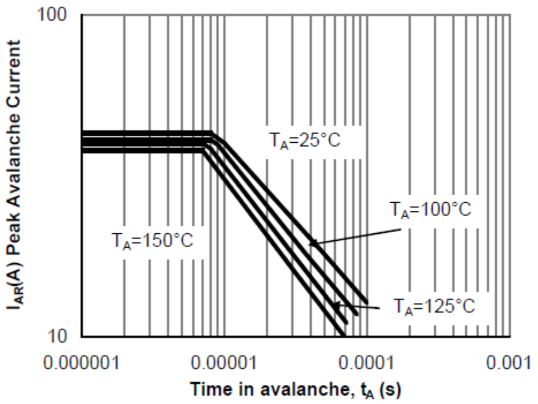


Figure 12: Single Pulse Avalanche capability (Note C)

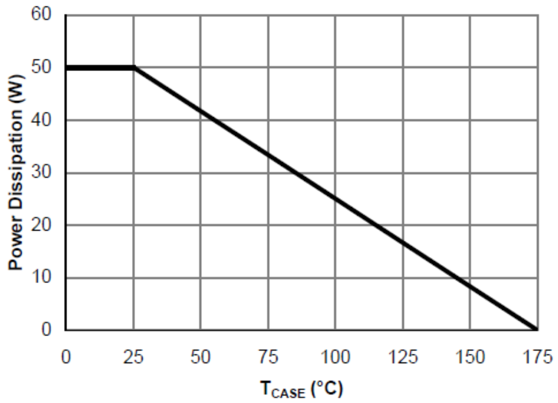


Figure 13: Power De-rating (Note F)

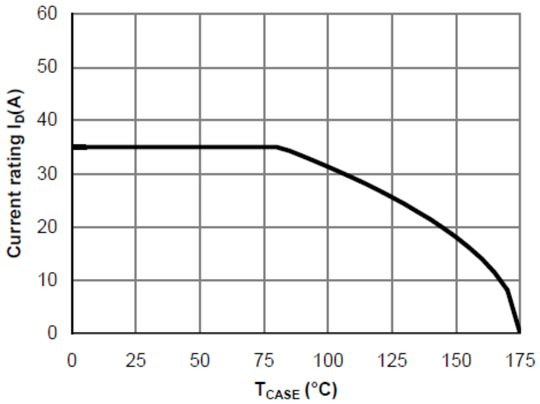


Figure 14: Current De-rating (Note F)

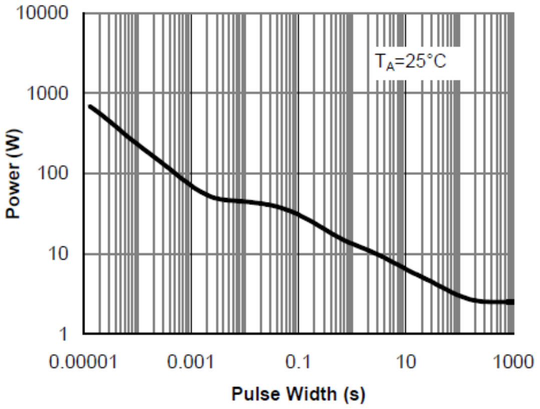


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

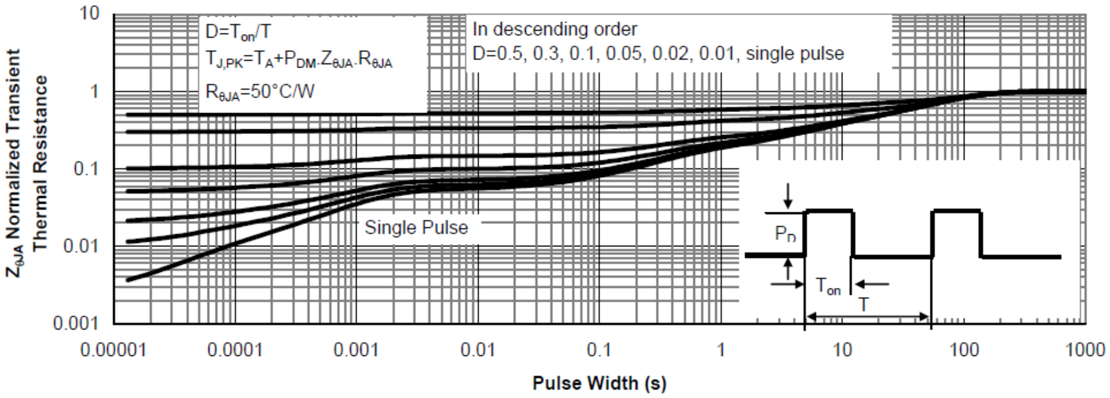
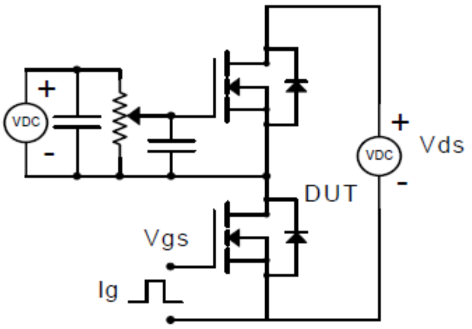
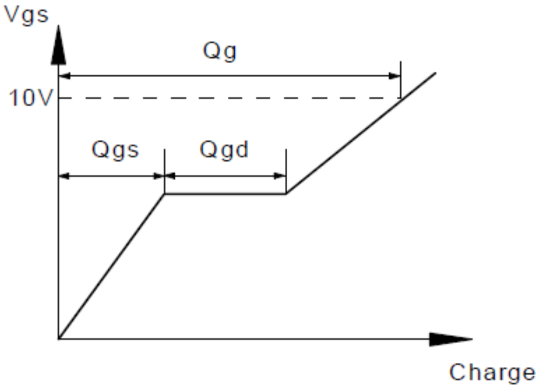


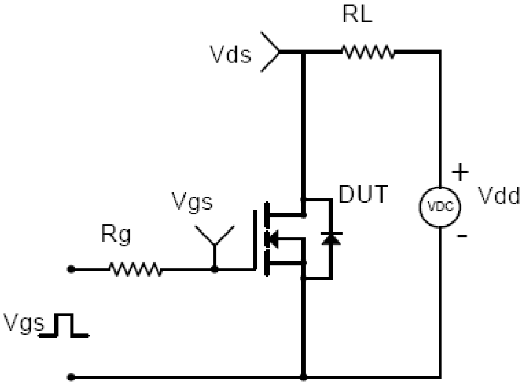
Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

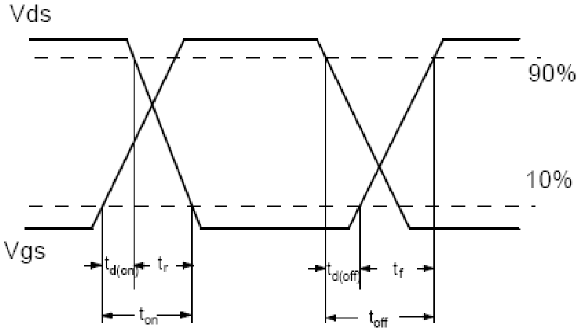
GATE CHARGE TEST CIRCUIT & WAVEFORM



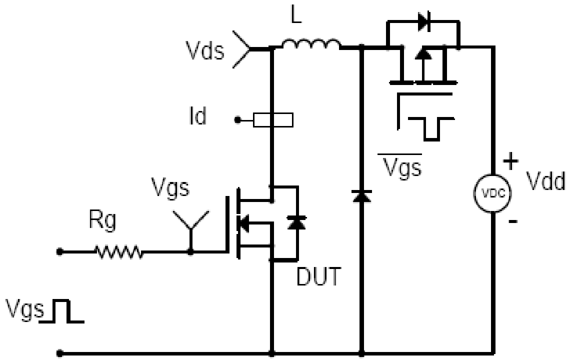


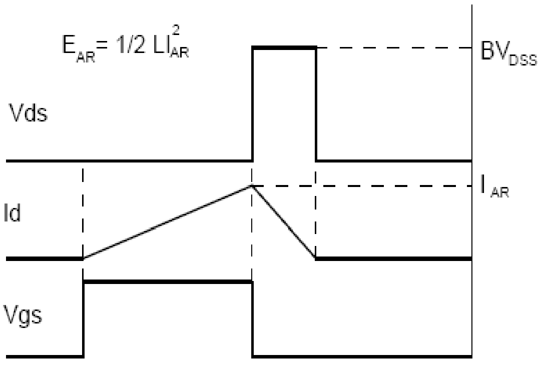
TESISTIVE SWITCHING TEST CIRCUIT & WAVEFORMS



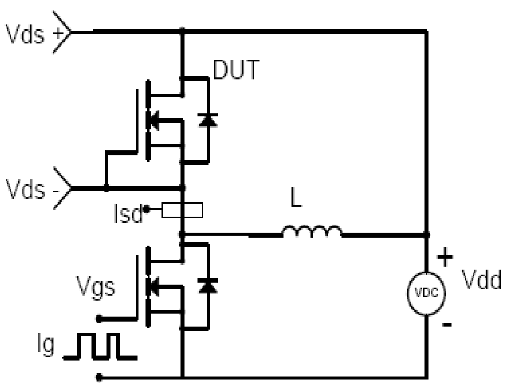


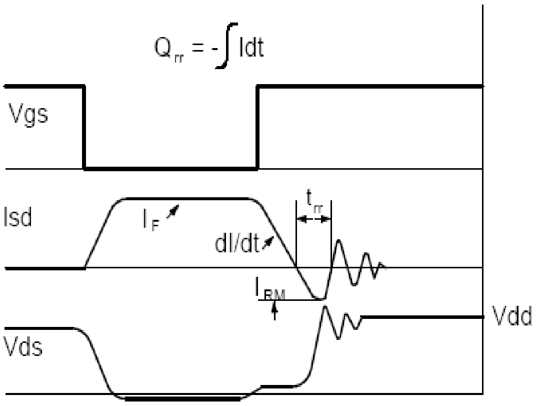
UNCLAMPED INDUCTIVE SWITCHING (UIS) TEST CIRCUIT & WAVEFORMS



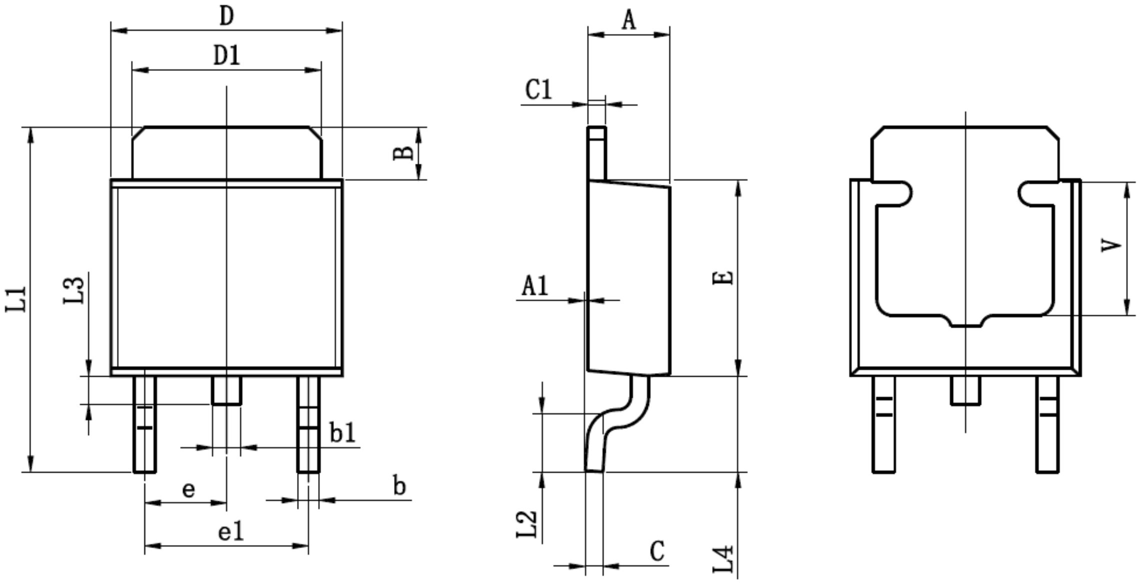


DIODE TEC0VERY TEST CIRCUIT & WAVEFORMS





TO-252-2L PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300TYP		0.091TYP	
e1	4.500	4.700	0.177	0.185
L1	9.500	9.900	0.374	0.390
L2	1.400	1.780	0.055	0.070
L3	0.650	0.950	0.026	0.037
L4	2.550	2.900	0.100	0.114
V	3.80REF		0.150REF	