STN4488L

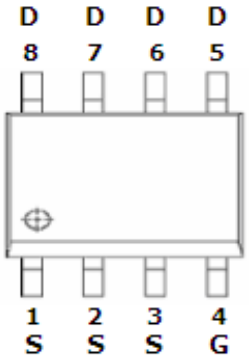
Dual N Channel Enhancement Mode MOSFET

20A

DESCRIPTION

STN4488L is the N-Channel logic enhancement mode power field effect transistors which are produced using high cell density DMOS trench technology. It is suitable for the power management applications in the portable or battery powered system.

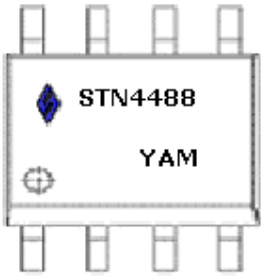
PIN CONFIGURATION
SOP-8

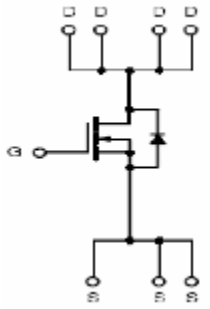


FEATURE

- **30V/20A, $R_{DS(ON)}$ = 3.8mΩ (Typ.) @VGS = 10V**
- **30V/18A, $R_{DS(ON)}$ = 5.2mΩ @VGS = 4.5V**
- **Super high density cell design for extremely low $R_{DS(ON)}$**
- **Exceptional on-resistance and maximum DC current capability**
- **SOP-8 package design**

PART MARKING
SOP-8





Y:Year Code A: Process Code

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ABSOULTE MAXIMUM RATINGS (Ta = 25℃ Unless otherwise noted)

Parameter		Symbol	10 Sec	Steady state	Unit
Drain-Source Voltage		V_{DSS}	30		V
Gate-Source Voltage		V_{GSS}	±20		V
Continuous Drain Current (TJ=150℃)	T_A=25℃	I_D	20	15	A
	T_A=70℃		17	12	
Pulsed Drain Current		I_{DM}	80		A
Continuous Source Current (Diode Conduction)		I_S	3.0		A
Power Dissipation	T_A=25℃	P_D	3.1	1.7	W
	T_A=70℃		20	1.1	
Operation Junction Temperature		T_J	-55/150		℃
Storgae Temperature Range		T_{STG}	-55/150		℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	Typ	Max	℃/W
			59	75	

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ELECTRICAL CHARACTERISTICS (Ta = 25℃ Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	1.0		2.5	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±10	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V,V_{GS}=0V			1	uA
		T_J=55℃			5	
On-State Drain Current	$I_{D(on)}$	V_{DS}=5V,V_{GS}=10V	80			A
Drain-source On-Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=20A		3.8	4.6	mΩ
		T_J=125°C		5.3	6.5	
		V_{GS}=4.5V, I_D=18A		5.2	6.4	
Forward Tran Conductance	g_{fs}	V_{DS}=10V,I_D=5.0A		72		S
Diode Forward Voltage	V_{SD}	I_S=8.0A,V_{GS}=0V			1.0	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=15V,V_{GS}=10V I_D=20A		84	112	nC
Gate-Source Charge	Q_{gs}			12		
Gate-Drain Charge	Q_{gd}			21		
Input Capacitance	Ciss	V_{DS}=15V,V_{GS}=0V f=1MHz		5450	6800	pF
Output Capacitance	Coss			760		
Reverse TransferCapacitance	Crss			540		
Turn-On Time	$t_{d(on)}$	V_{DS}=15V,R_L=0.75Ω I_D=1A,V_G=10V R_G=3.0Ω		13		nS
	tr			9.8		
Turn-Off Time	$t_{d(off)}$			49		
	tf			16		

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TYPICAL CHARACTERICTICS

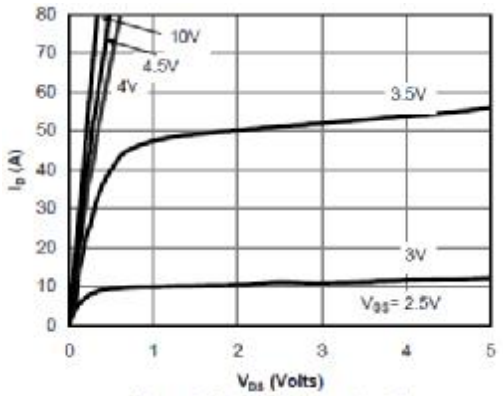

Figure 1: On-Region Characteristics

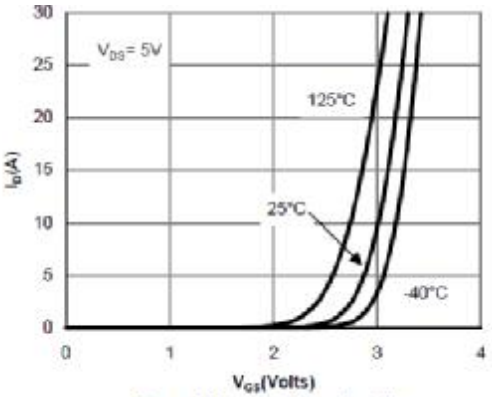

Figure 2: Transfer Characteristics

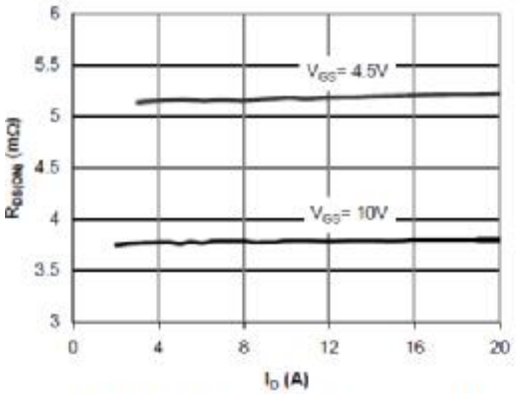

Figure 3: On-Resistance vs. Drain Current and Gate Voltage

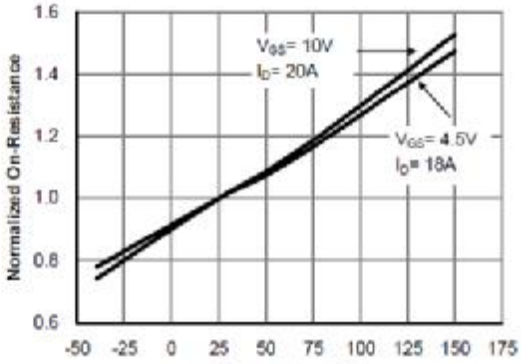

Figure 4: On-Resistance vs. Junction Temperature

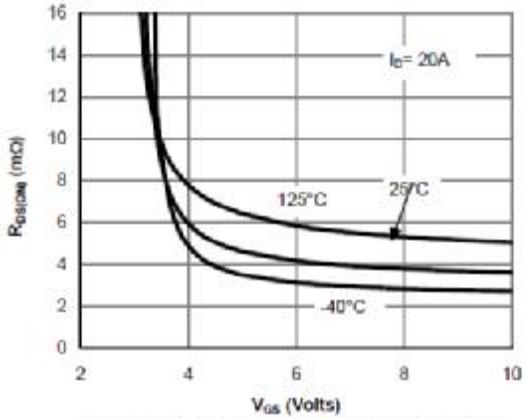

Figure 5: On-Resistance vs. Gate-Source Voltage

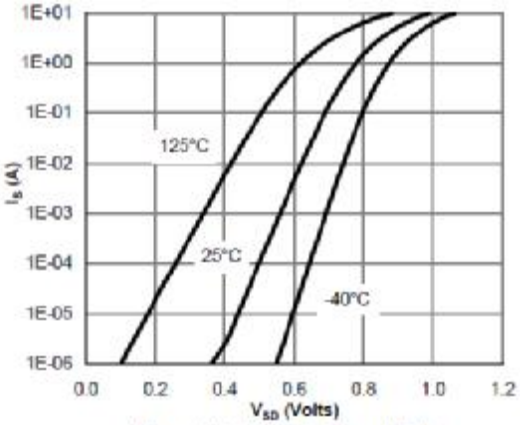

Figure 6: Body-Diode Characteristics

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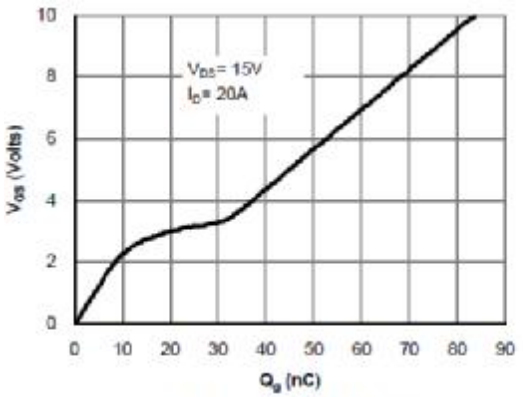

Figure 7: Gate-Charge Characteristics

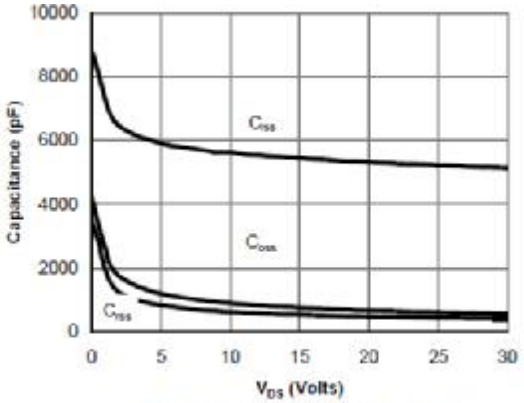

Figure 8: Capacitance Characteristics

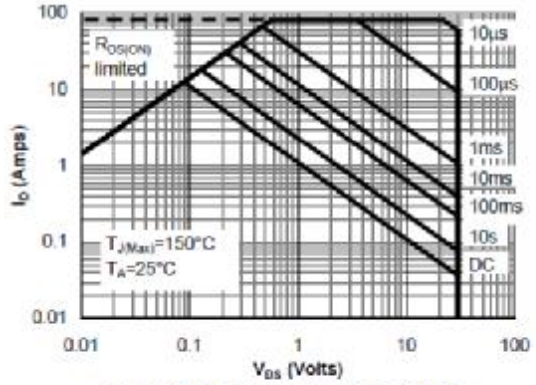

Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

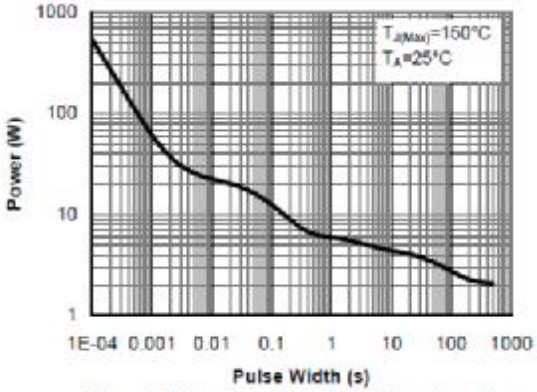

Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

TYPICAL CHARACTERICTICS

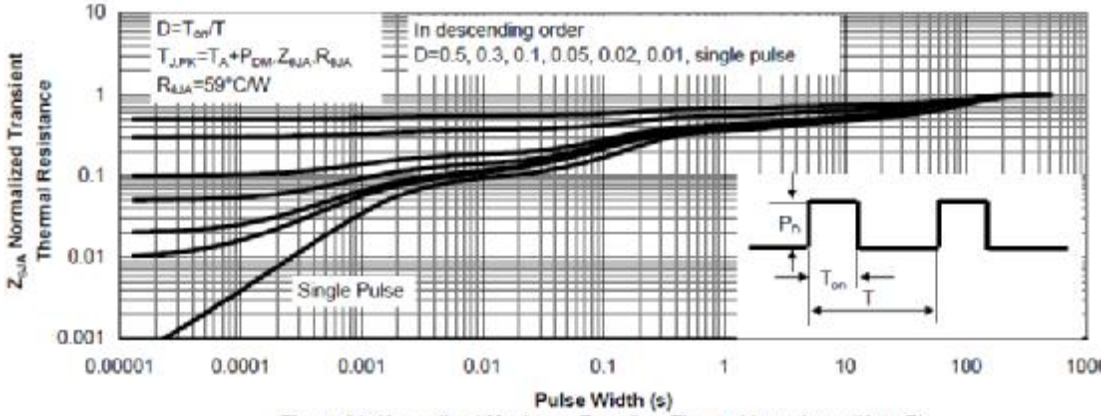

Figure 11: Normalized Maximum Transient Thermal Impedance(Note E)

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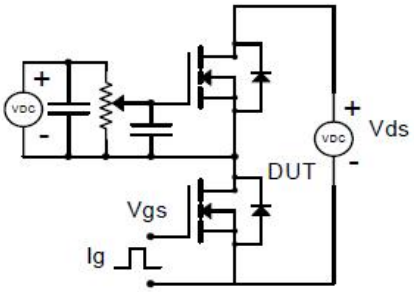
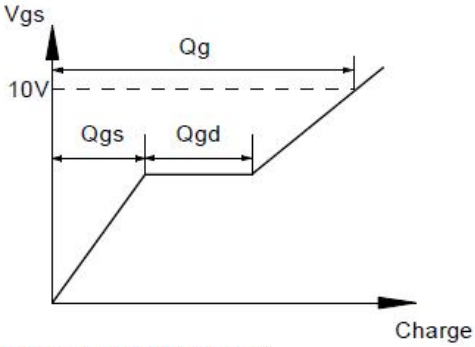
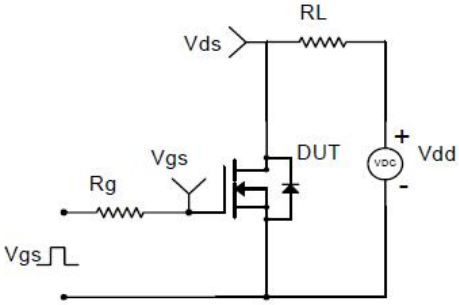
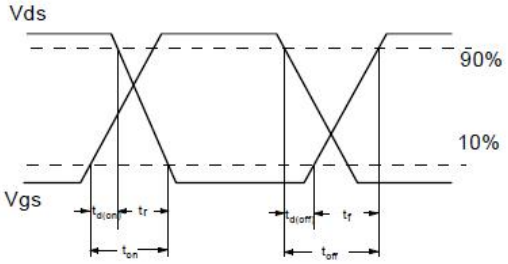
Gate Charge Test Circuit & Waveform



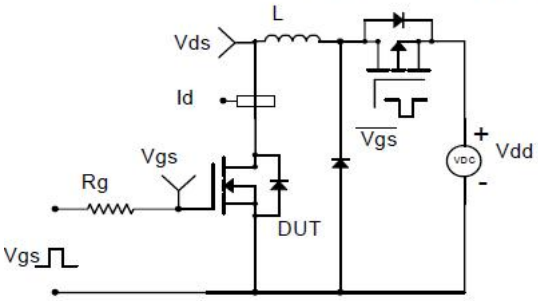


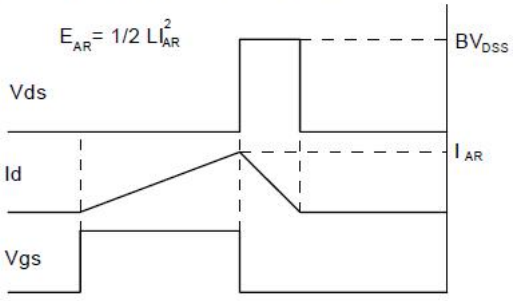
Resistive Switching Test Circuit & Waveforms



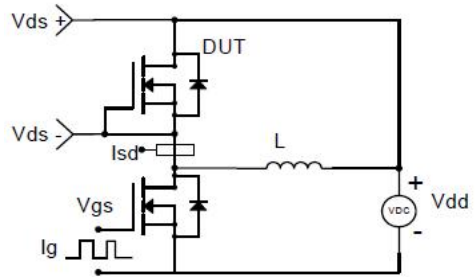


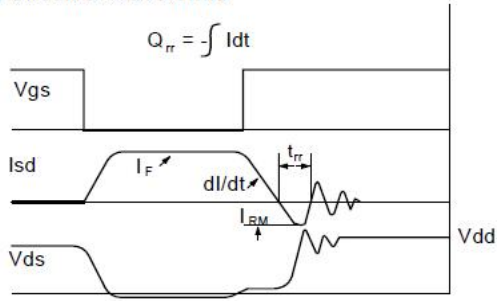
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms





Diode Recovery Test Circuit & Waveforms





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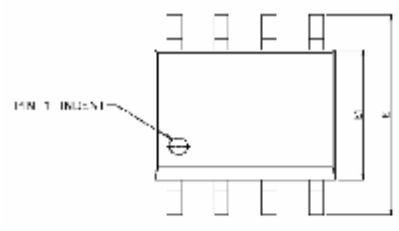
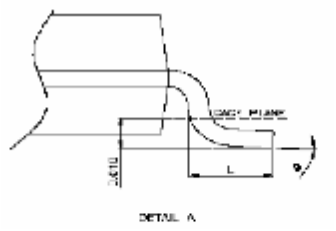
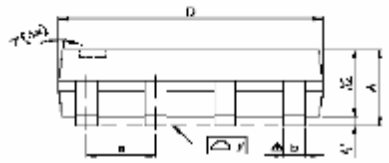
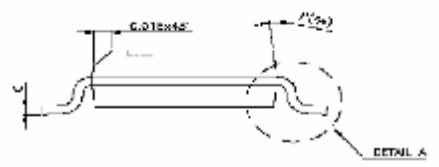
SOP-8 PACKAGE OUTLINE









SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	——	0.25	0.004	——	0.010
A2	——	1.45	——	——	0.057	——
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	——	1.27	——	——	0.050	——
L	0.38	0.71	1.27	0.015	0.028	0.050
⚠ y	——	——	0.076	——	——	0.003
θ	0°	——	8°	0°	——	8°

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