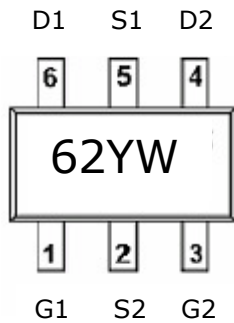


DESCRIPTION

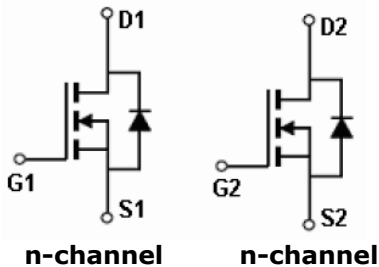
The STN6562 is the dual N-Channel enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

**PIN CONFIGURATION
TSOP-6**


Y: Year
A: Week Code

FEATURE

- ◆ 30V/4.0A, $R_{DS(ON)}=65\text{mohm}@V_{GS}=10\text{V}$
- ◆ 30V/2.2A, $R_{DS(ON)}=75\text{mohm}@V_{GS}=4.5\text{V}$
- ◆ 30V/1.5A, $R_{DS(ON)}=105\text{mohm}@V_{GS}=2.5\text{V}$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional an-resistance and maximum DC current capability
- ◆ TSOP-6 package design





STN6562  Lead-free

Dual N Channel Enhancement Mode MOSFET
4.0A

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V _{DSS}	30	V
Gate-Source Voltage		V _{GSS}	±20	V
Continuous Drain Current (T _J =150°C)	T _A =25°C	I _D	4.0	A
	T _A =70°C		2.0	
Pulsed Drain Current		I _{DM}	20	A
Continuous Source Current (Diode Conduction)		I _S	1.7	A
Power Dissipation	T _A =25°C	P _D	2.0	W
	T _A =70°C		1.3	
Operation Junction Temperature		T _J	-55/150	°C
Storage Temperature Range		T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient	T ≤ 10sec	R _{θJA}	50	°C/W
	Steady State			



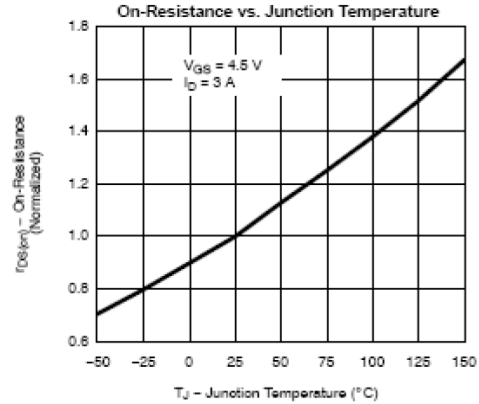
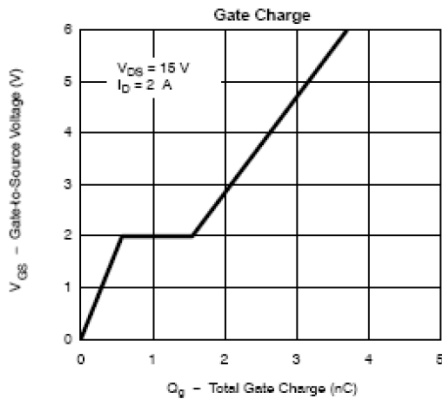
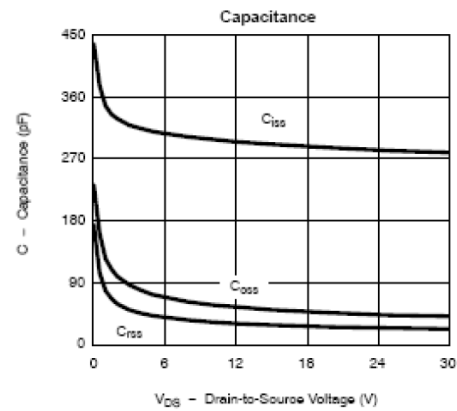
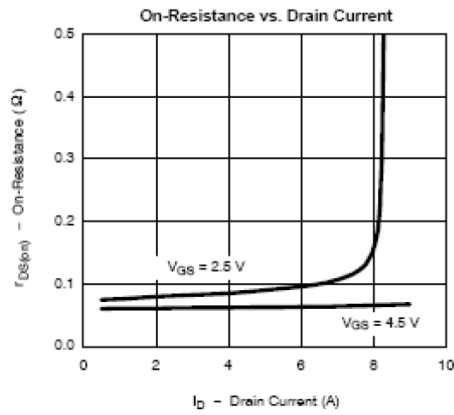
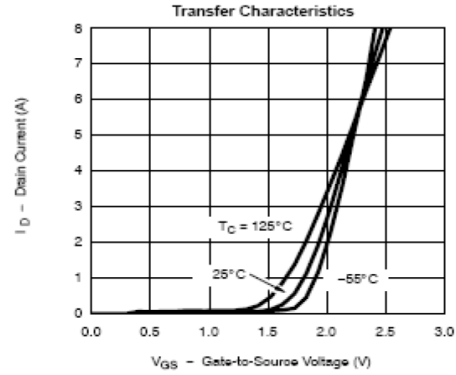
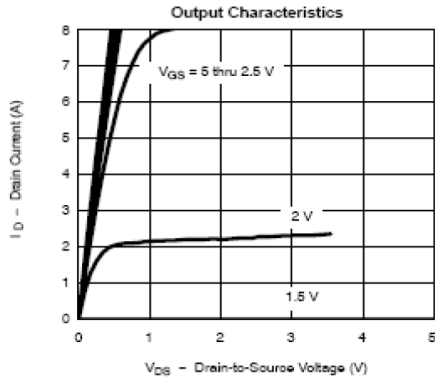
STN6562 

Dual N Channel Enhancement Mode MOSFET
4.0A

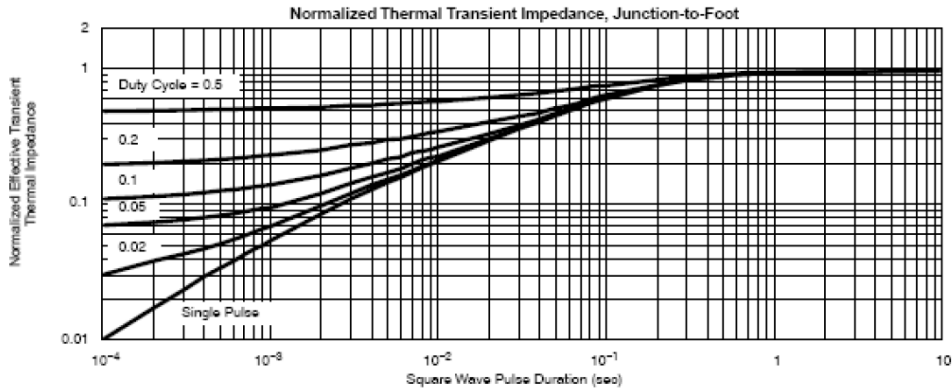
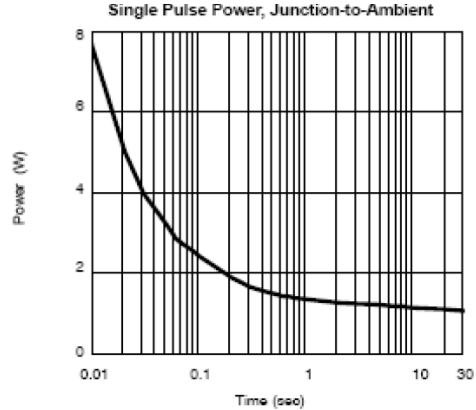
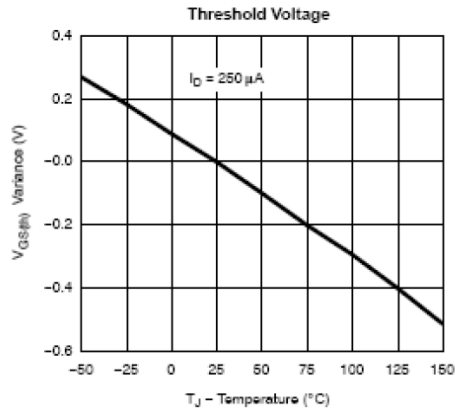
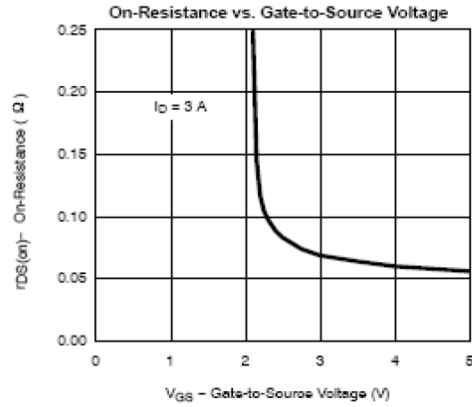
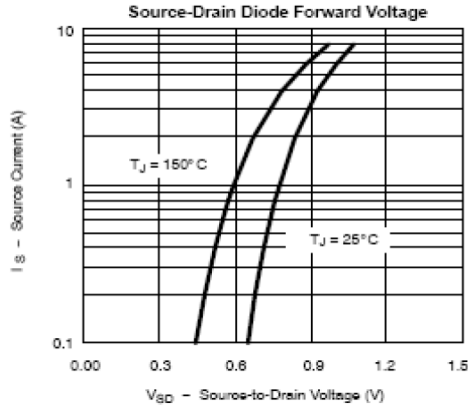
ELECTRICAL CHARACTERISTICS (Ta = 25°C Unless otherwise noted)

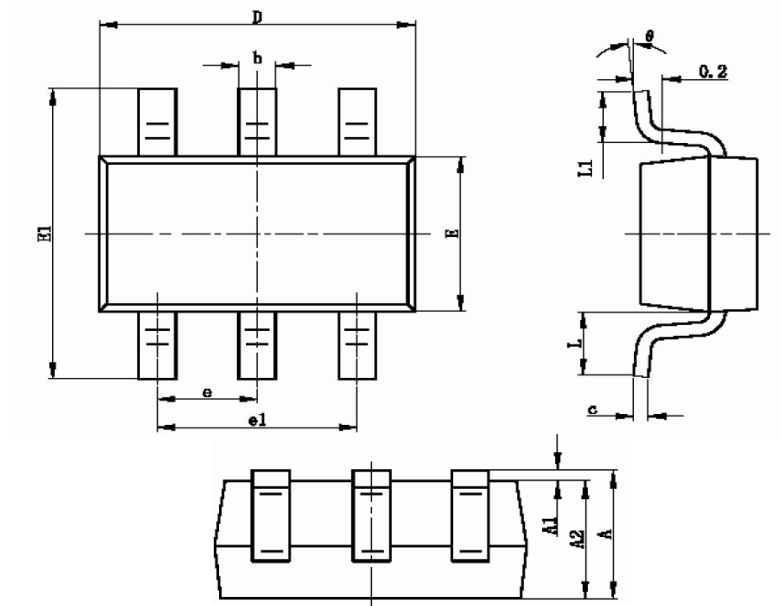
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.8		1.6	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=24V, V_{GS}=0V$			1	uA
		$V_{DS}=24V, V_{GS}=0V$ $T_J=55^\circ C$			10	
On-State Drain Current	$I_{D(on)}$	$V_{DS}\geq 5V, V_{GS}=10V$	30			A
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=2.8A$		0.056	0.065	Ω
		$V_{GS}=4.5V, I_D=2.3A$		0.068	0.075	
		$V_{GS}=2.5V, I_D=1.8A$		0.097	0.105	
Forward Transconductance	g_{fs}	$V_{DS}=4.5V, I_D=2.5A$		4.6		S
Diode Forward Voltage	V_{SD}	$I_S=1.25A, V_{GS}=0V$			1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=15V, V_{GS}=4.5V,$ $V_{DS}=2.0A$		4.2	6	nC
Gate-Source Charge	Q_{gs}			0.6		
Gate-Drain Charge	Q_{gd}			1.7		
Input Capacitance	C_{iss}	$V_{DS}=15V, V_{GS}=0,$ $f=1MHz$		340		pF
Output Capacitance	C_{oss}			55		
Reverse Transfer Capacitance	C_{rss}			41		
Turn-On Time	$T_{d(on)}$	$V_{DD}=15V,$ $R_L=15\Omega, V_{GEN}=10V,$ $R_G=3\Omega$		2.5		ns
	t_r			2.5		
Turn-Off Time	$T_{d(off)}$			20		
	t_f			4		

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS



TSOP-6 PACKAGE OUTLINE


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°