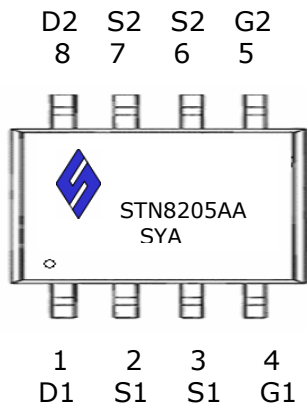


DESCRIPTION

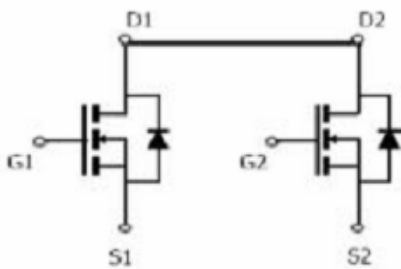
STN8205AA is the dual N-Channel enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, such as notebook computer power management and other battery powered circuits, where high-side switching is required.

PIN CONFIGURATION
TSSOP-8


S : Subcontractor
Y: Year
A: Week Code

FEATURE

- 20V/6.0A, $R_{DS(ON)} = 30\text{m-ohm}@V_{GS} = 4.5\text{V}$
- 20V/5.0A, $R_{DS(ON)} = 42\text{m-ohm}@V_{GS} = 2.5\text{V}$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional low on-resistance and maximum DC current capability
- TSSOP-8 package design


ORDERING INFORMATION

Part Number	Package	Part Marking
STN8205AAST8RG	TSSOP-8	SYA

Week Code Code : A ~ Z(1~26) ; a ~ z(27~52)

ST8205AAST8RG ST8 : TSSOP-8; R: Tape Reel ; G: Pb - Free



STN8205AA



Dual N Channel Enhancement Mode MOSFET

6.0A

ABSOLUTE MAXIMUM RATINGS (Ta = 25 unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V _{DSS}	20	V
Gate-Source Voltage		V _{GSS}	+/-20	V
Continuous Drain Current (T _J =150)	T _A =25	I _D	6.0	A
	T _A =70		3.4	
Pulsed Drain Current		I _{DM}	30	A
Continuous Source Current (Diode Conduction)		I _S	2	A
Power Dissipation	T _A =25	P _D	2.0	W
	T _A =70		1.2	
Operation Junction Temperature		T _J	-40/140	
Storage Temperature Range		T _{STG}	-55/150	
Thermal Resistance-Junction to Ambient		R _{θJA}	105	/W



STN8205AA



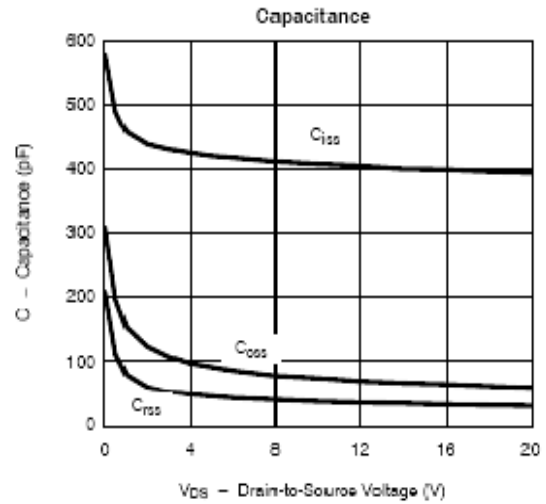
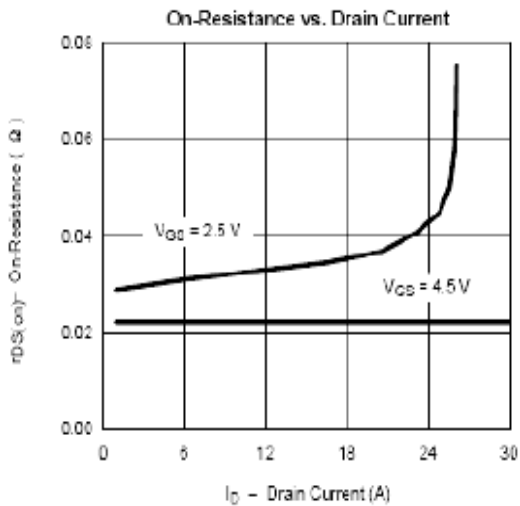
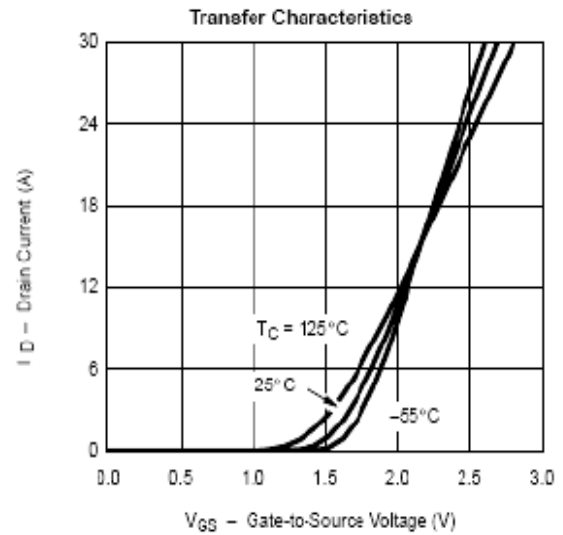
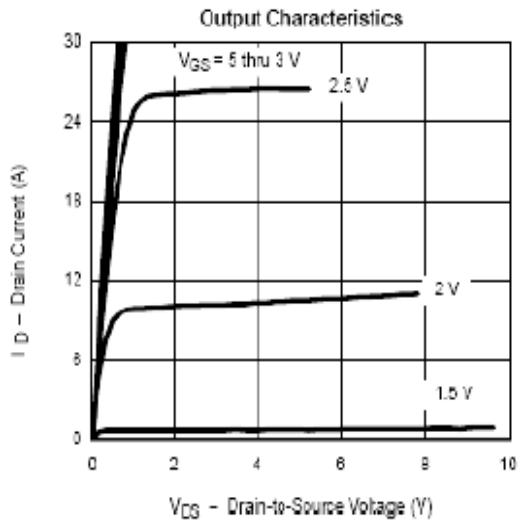
Dual N Channel Enhancement Mode MOSFET

6.0A

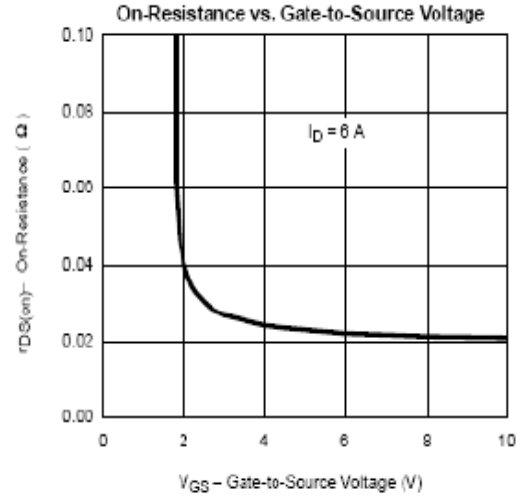
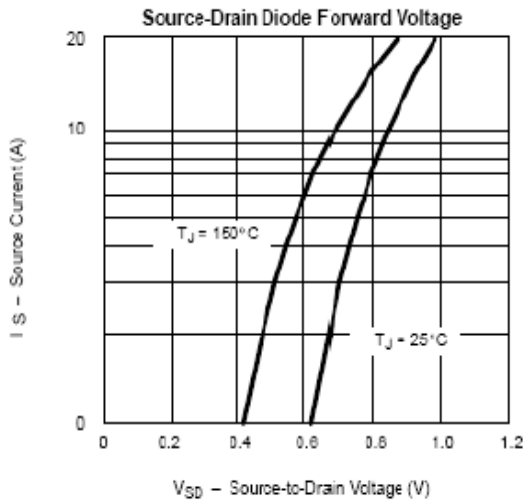
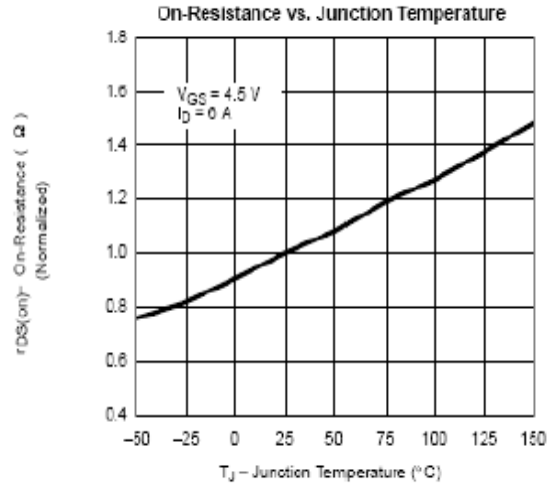
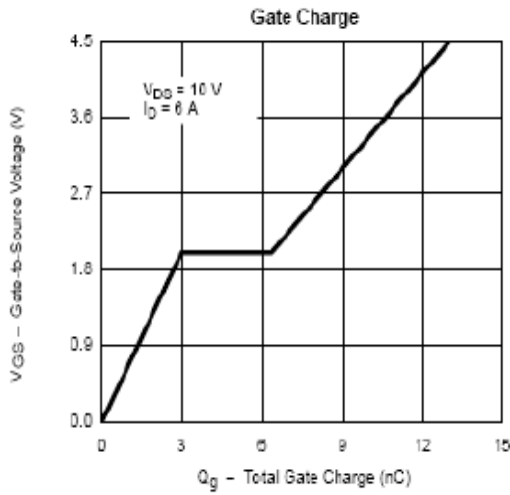
ELECTRICAL CHARACTERISTICS (Ta = 25 unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	20			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.6		1.2	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=+/-20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=20V, V_{GS}=0V$			1	uA
		$V_{DS}=20V, V_{GS}=0V$ $T_J=85$			5	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \le 5V, V_{GS}=4.5V$	6			A
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=6.0A$		0.024	0.030	Ω
		$V_{GS}=2.5V, I_D=5.0A$		0.032	0.042	
Forward Transconductance	g_{fs}	$V_{DS}=5V, I_D=3.6A$		10		S
Diode Forward Voltage	V_{SD}	$I_S=1.7A, V_{GS}=0V$		0.8	1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=10V, V_{GS}=4.5V, V_{DS}=4A$		10.5		nC
Gate-Source Charge	Q_{gs}			2.5		
Gate-Drain Charge	Q_{gd}			2.1		
Input Capacitance	C_{iss}	$V_{DS}=8V, V_{GS}=0V$ $f=1MHz$		805		pF
Output Capacitance	C_{oss}			155		
Reverse Transfer Capacitance	C_{rss}			122		
Turn-On Time	$T_{d(on)}$	$V_{DD}=10V, R_L=10\Omega, I_D=1.0A,$ $V_{GEN}=4.5V, R_G=10\Omega$		14		nS
	t_r			6		
Turn-Off Time	$T_{d(off)}$			45		
	t_f			20		

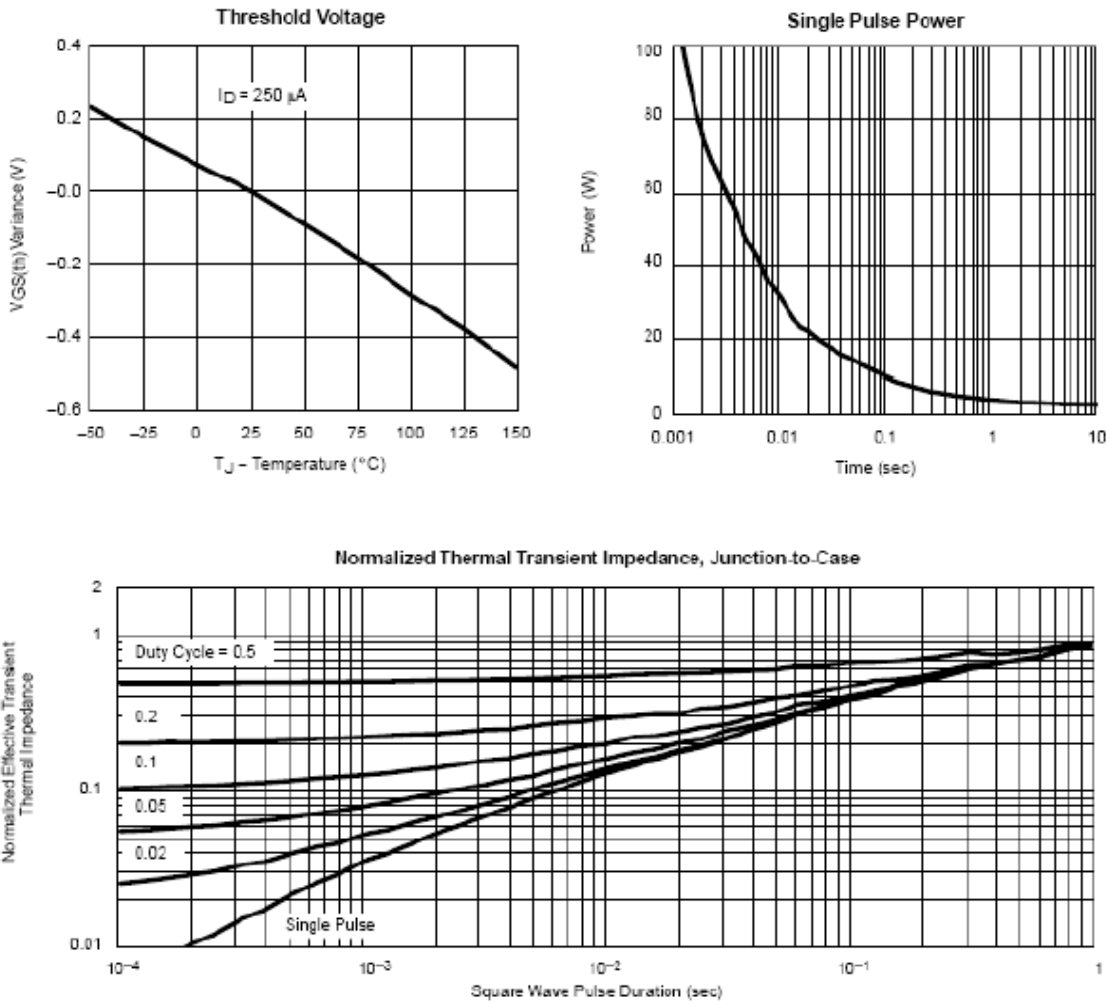
TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS



TSSOP-8 PACKAGE OUTLINE

