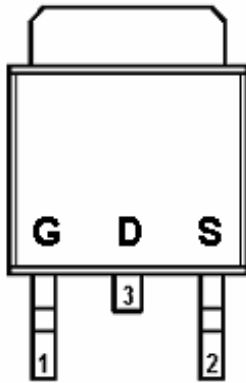


DESCRIPTION

STP601D is the P-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. The STP401 has been designed specially to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

**PIN CONFIGURATION
TO-252-2L**



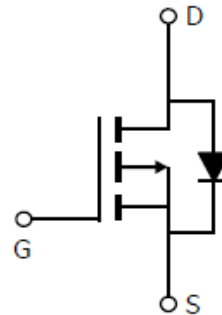
PART MARKING



Y : Year Code
A : Date Code
B : Process Code
C : package Code

FEATURE

- -60V/-20.0A, $R_{DS(ON)} = 20m\Omega$
@ $V_{GS} = -10V$
- -60V/-20.0A, $R_{DS(ON)} = 35m\Omega$
@ $V_{GS} = -4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- TO-252 package design





ABSOLUTE MAXIMUM RATINGS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	VDSS	-60	V
Gate-Source Voltage	VGSS	±20	V
Continuous Drain Current (TJ=150°C)	ID	-30.0 -20.0	A
Pulsed Drain Current	IDM	-80	A
Single Pulse Avalanche Energy	EAS	113	mJ
Power Dissipation	PD	52	W
Operation Junction Temperature	TJ	150	°C
Storage Temperature Range	TSTG	-55/150	°C
Thermal Resistance-Junction to Case	RθJC	2.4	°C/W



STP601D



P Channel Enhancement Mode MOSFET

-30A

ELECTRICAL CHARACTERISTICS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.0		-2.5	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-48V, V_{GS}=0V$			-1	uA
		$V_{DS}=-48V, V_{GS}=0V$ $T_J=55^\circ C$			-5	
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-20A$ $V_{GS}=-4.5V, I_D=-20A$		22 28	30 35	mΩ
Forward Transconductance	g_{fs}	$V_{DS}=-50V, I_D=-18A$	23			S
Diode Forward Voltage	V_{SD}	$I_S=-1.0A, V_{GS}=0V$			-1	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=-20V, V_{GS}=-4.5V$ $I_D=-12A$		25		nC
Gate-Source Charge	Q_{gs}			6.7		
Gate-Drain Charge	Q_{gd}			5.5		
Input Capacitance	C_{iss}	$V_{DS}=-15V, V_{GS}=0V$ $F=1MHz$		3600		pF
Output Capacitance	C_{oss}			140		
Reverse Transfer Capacitance	C_{rss}			153		
Turn-On Time	$t_{d(on)}$	$V_{GS}=-15V, I_D=-1A$ $V_{GEN}=10V, R_G=3.3\Omega$		38		nS
	t_r			24		
Turn-Off Time	$t_{d(off)}$			100		
	t_f			7		

TYPICAL CHARACTERISTICS

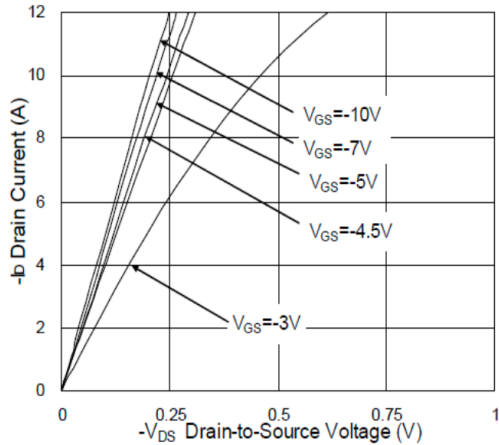


Fig 1. Output Characteristic

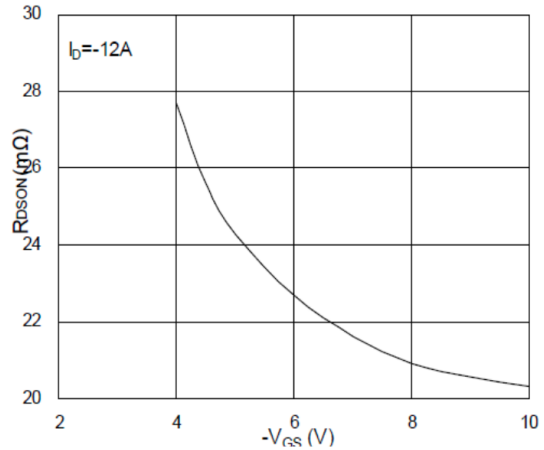


Fig 2. On Resistance vs Gate Source Voltage

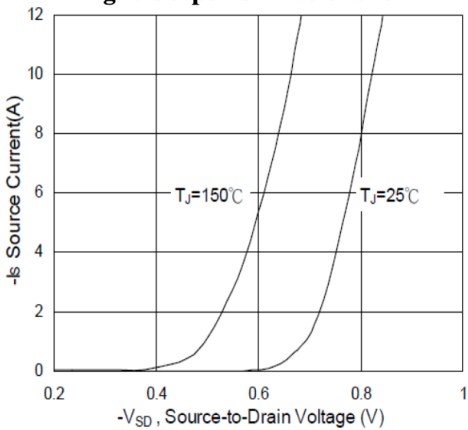


Fig 3. Source-Drain Diode Forward Voltage

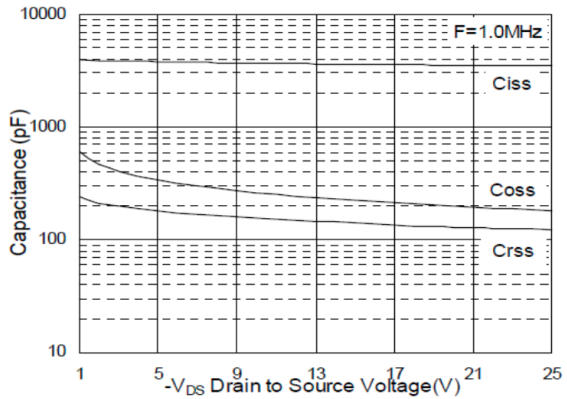


Fig 4. Capacitance

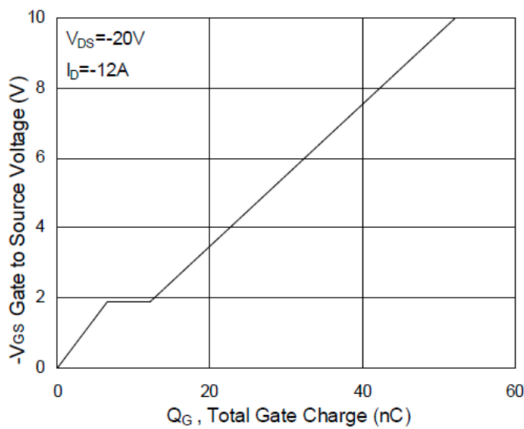


Fig 5. Gate Charge

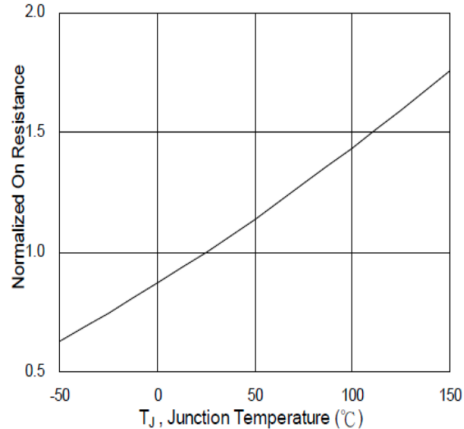


Fig 6. On Resistance vs Junction Temperature

TYPICAL CHARACTERISTICS

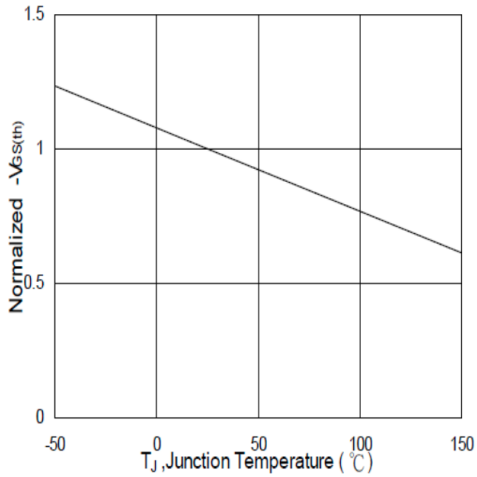


Fig. 7 Threshold Voltage vs Temperature

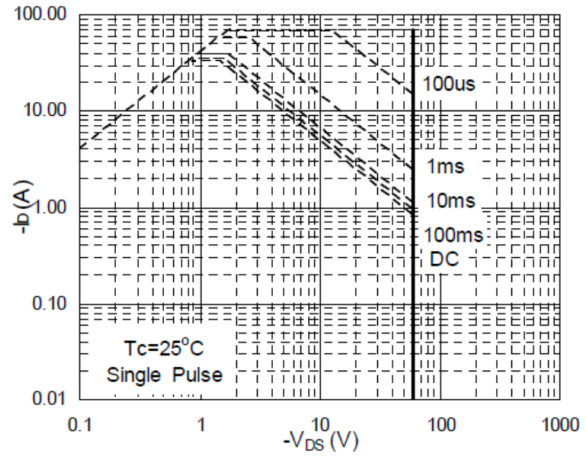


Fig. 8 Safe Operating Rnage

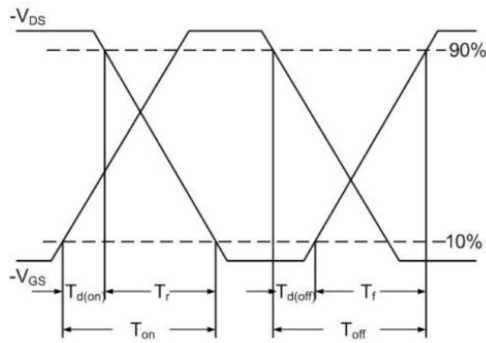


Fig. 9. Switching Time Waveform

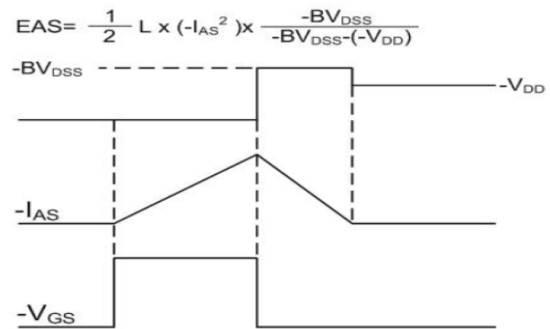


Fig. 10 Unclamped Inductive Waveform

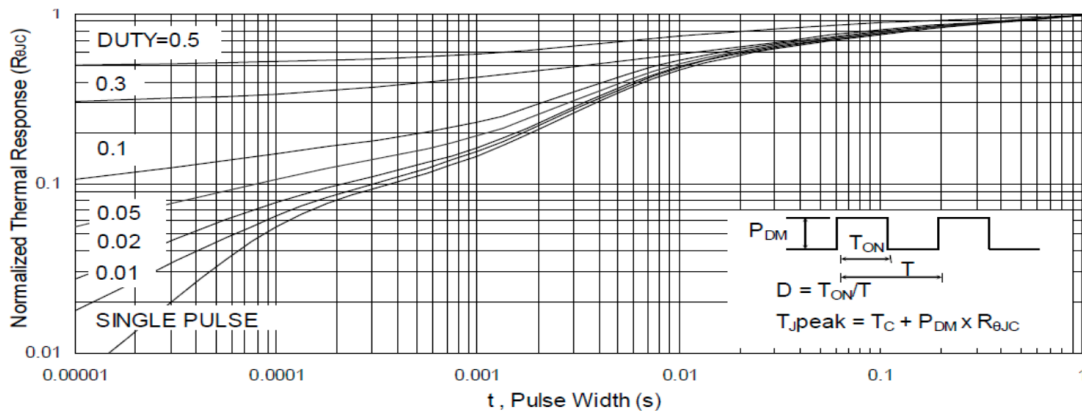
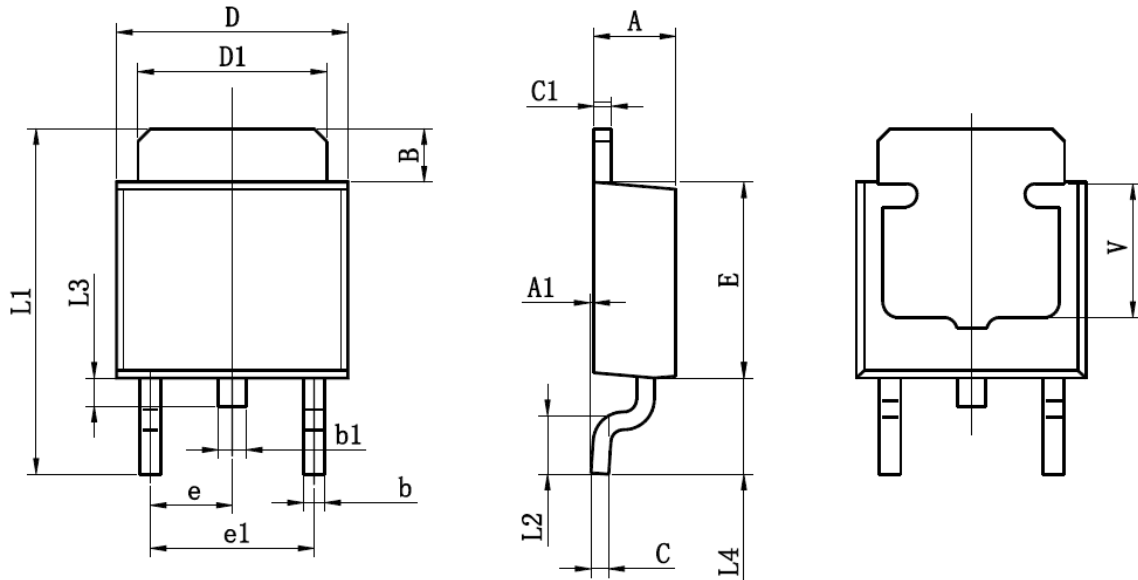


Fig. 11. Maximum Transient Thermal Impedance

TO-252-2L PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300TYP		0.091TYP	
e1	4.500	4.700	0.177	0.185
L1	9.500	9.900	0.374	0.390
L2	1.400	1.780	0.055	0.070
L3	0.650	0.950	0.026	0.037
L4	2.550	2.900	0.100	0.114
V	3.80REF		0.150REF	