STANSON

STP9527

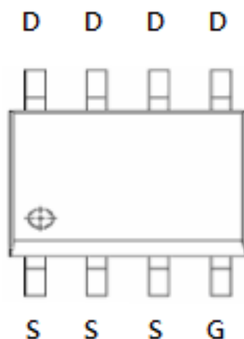
P Channel Enhancement Mode MOSFET

-10.0A

suSCRIPTION

STP9527 is the P-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, noteook power management ane ther battery powered circuits where high-side witching.

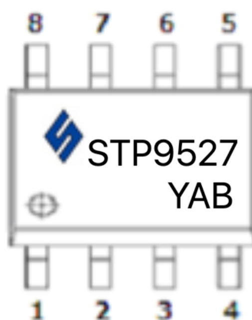
PIN CONFIGURATION
SOP-8

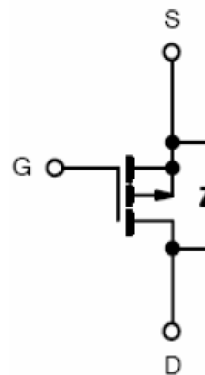


FEATURE

- -40V/-10.0A, $R_{DS(ON)}$ = 32mΩ (Typ.) @V_{GS} =-10V
- -40V/-8.0A, $R_{DS(ON)}$ = 38mΩ @V_{GS} = -4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOP-8 package design

PART MARKING
SOP-8





Y : Year Code
A : Date Code
B : Wafer Code

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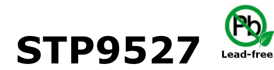

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ABSOULTE MAXIMUM RATINGS (Ta = 25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	-40	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current (TJ=150℃)	T_A=25℃ T_A=70℃	I_D	-10.0 -8.0	A
Pulsed Drain Current		I_{DM}	-30	A
Continuous Source Current (Diode Conduction)		I_S	-2.3	A
Power Dissipation	T_A=25℃ T_A=70℃	P_D	2.8 1.8	W
Operation Junction Temperature		T_J	-55/150	℃
Storgae Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	70	℃/W

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ELECTRICAL CHARACTERISTICS (Ta = 25℃ Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=-250uA	-40			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250 uA	-0.8		-2.5	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-36V,V_{GS}=0V			-1	uA
		V_{DS}=-36V,V_{GS}=0V T_J=85℃			-10	
On-State Drain Current	$I_{D(on)}$	V_{DS}=-5V,V_{GS}=4.5	-10			A
Drain-source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V, I_D=-10A V_{GS}=-4.5V, I_D=-8A		0.032 0.038	0.040 0.050	Ω
Forward Tran Conductance	gfs	V_{DS}=-15V,I_D=-5.7A		13		S
Diode Forward Voltage	V_{SD}	I_S=-2.3A,V_{GS}=0V		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=-20V,V_{GS}=-4.5 I_D≡-5.0A		13	20	nC
Gate-Source Charge	Q_{gs}			4.5		
Gate-Drain Charge	Q_{gd}			6.5		
Input Capacitance	Ciss	V_{DS} =-20V,VGS=0V f=1MHz		1100		pF
Output Capacitance	Coss			145		
Reverse TransferCapacitance	Crss			115		
Turn-On Time	$t_{d(on)}$	V_{DD}=20V,R_L=4Ω I_D=-5.0A,V_{GEN}=-4.5 R_G=1Ω		40	80	nS
	t_r			55	100	
Turn-Off Time	$t_{d(off)}$			30	60	
	t_f			12	20	

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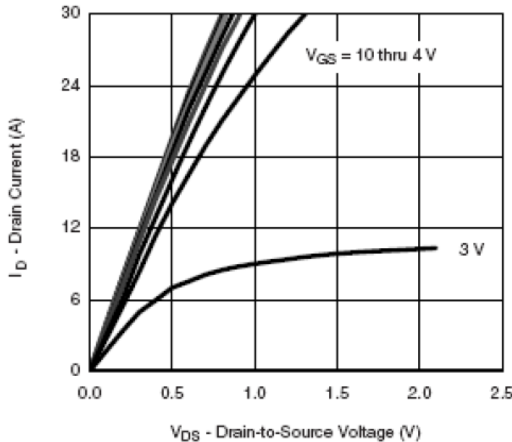
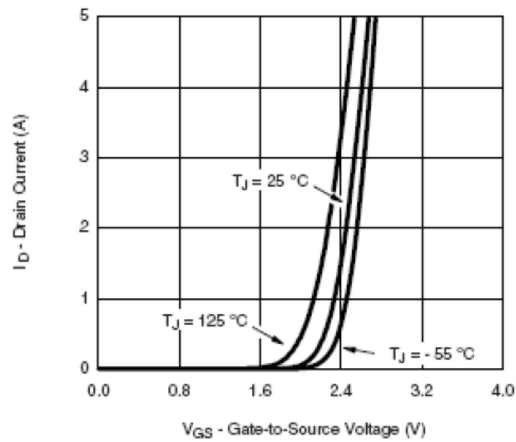
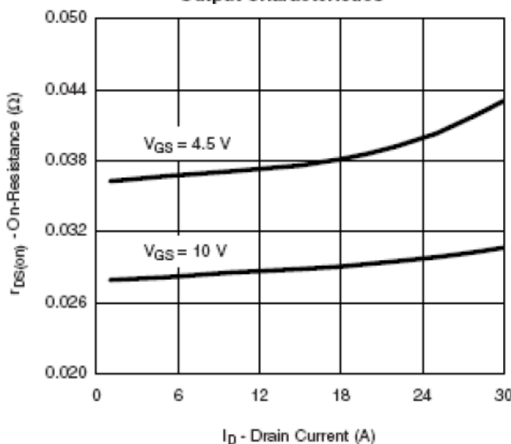
TYPICAL CHARACTERICTICS



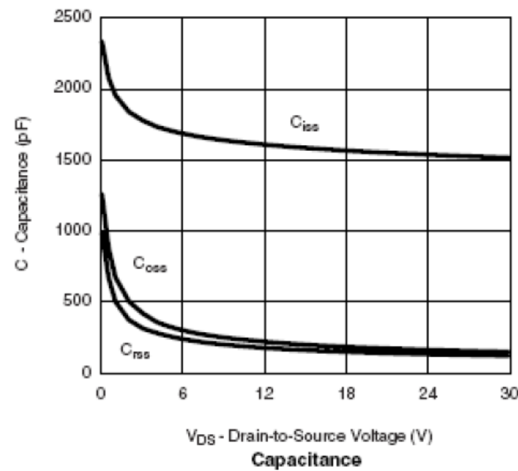
Output Characteristics



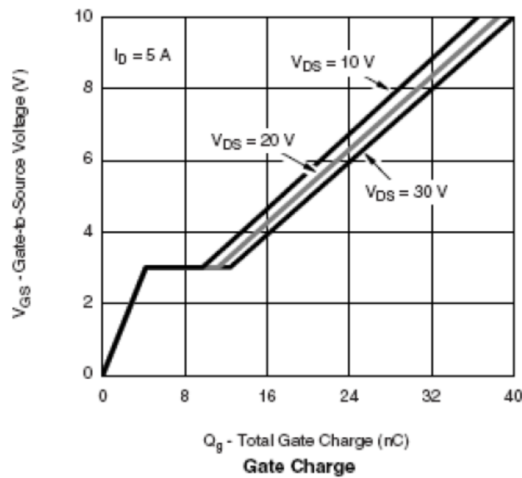
Transfer Characteristics



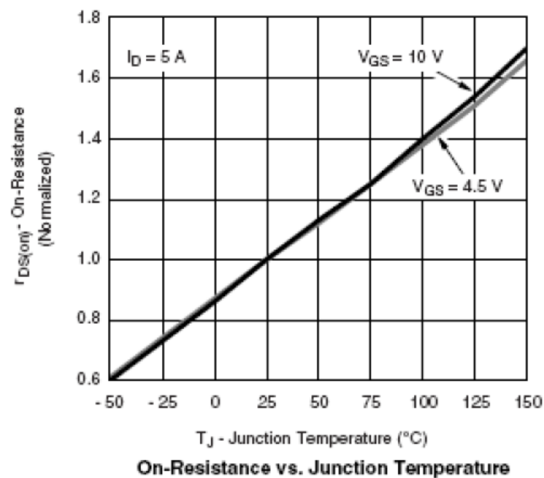
On-Resistance vs. Drain Current



Capacitance



Gate Charge



On-Resistance vs. Junction Temperature

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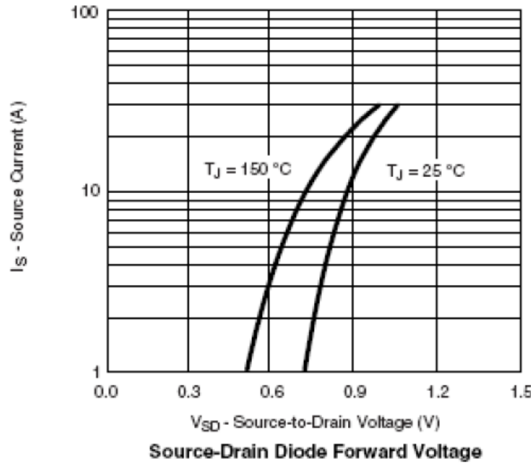
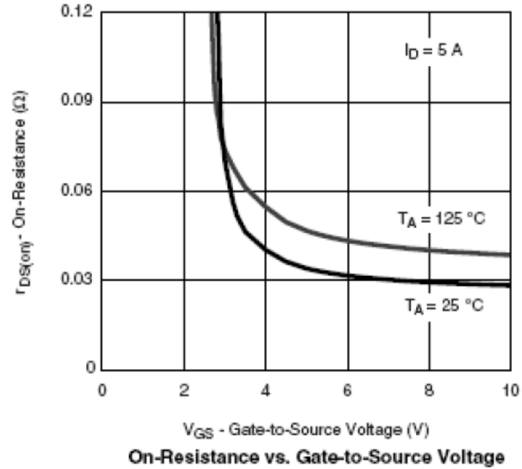
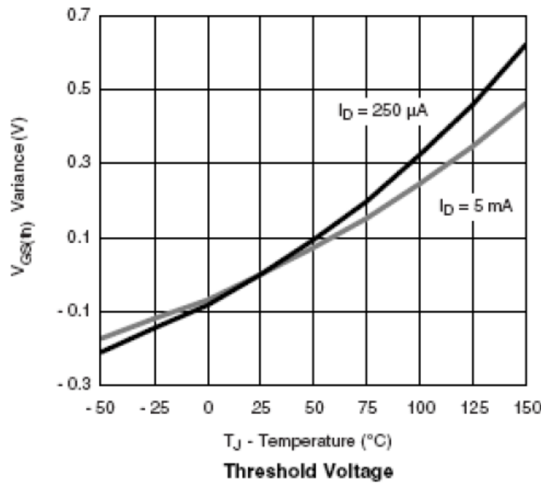
TYPICAL CHARACTERICTICS



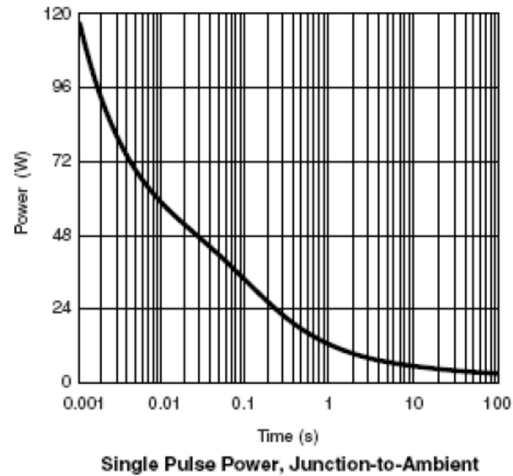
Source-Drain Diode Forward Voltage



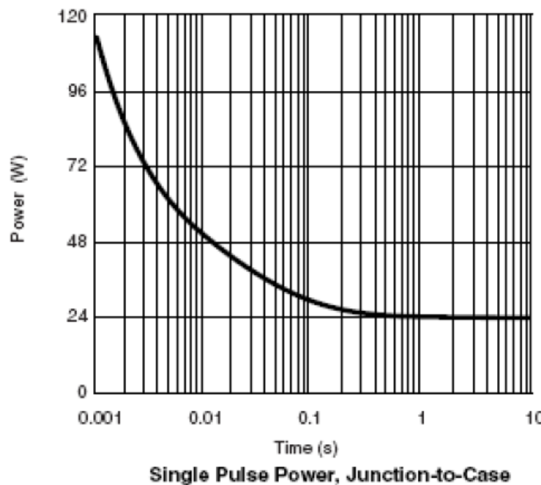
On-Resistance vs. Gate-to-Source Voltage



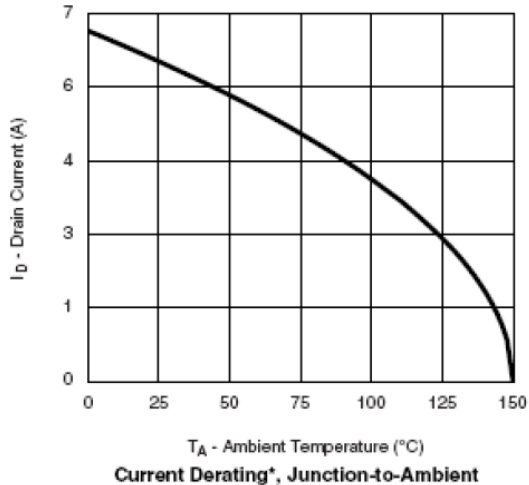
Threshold Voltage



Single Pulse Power, Junction-to-Ambient



Single Pulse Power, Junction-to-Case



Current Derating*, Junction-to-Ambient

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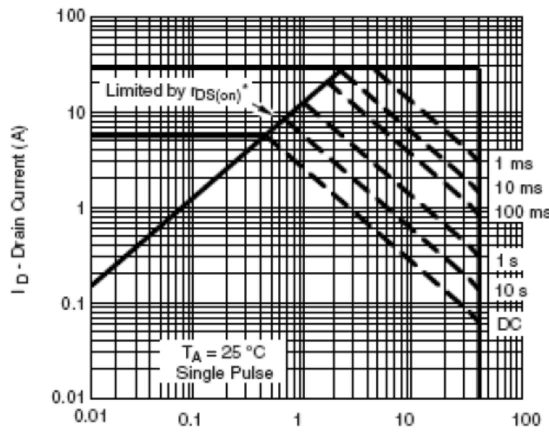
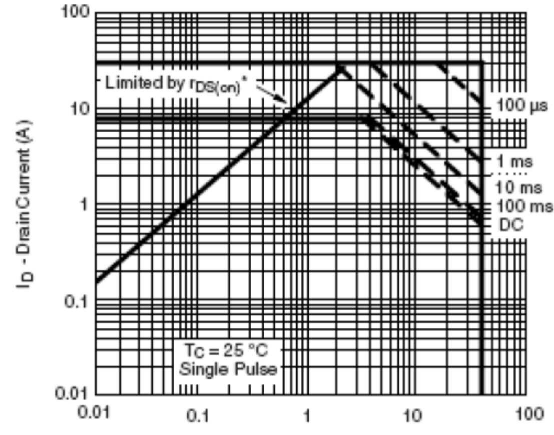
TYPICAL CHARACTERICTICS



* V_{GS} > minimum V_{GS} at which $r_{DS(on)}$ is specified

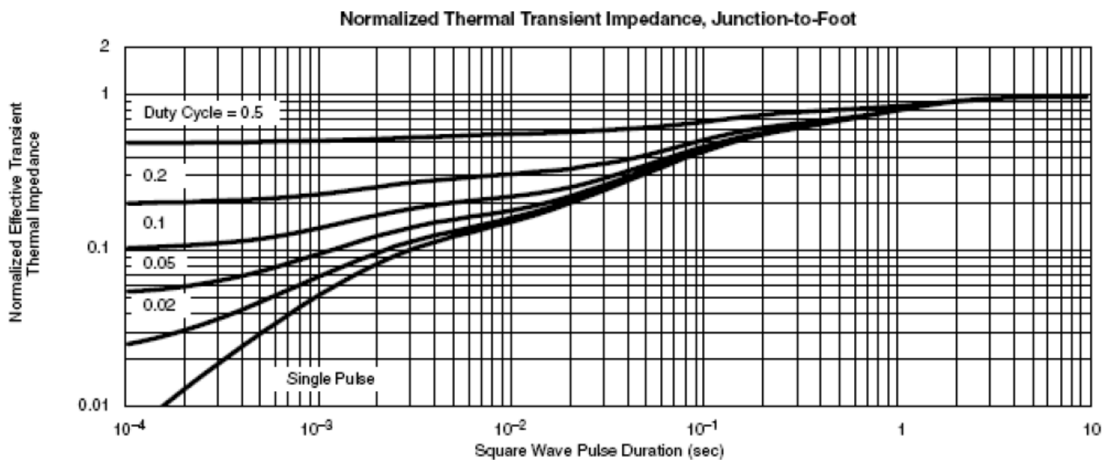
Safe Operating Area, Junction-to-Ambient



* V_{GS} > minimum V_{GS} at which $r_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Case

Normalized Thermal Transient Impedance, Junction-to-Foot



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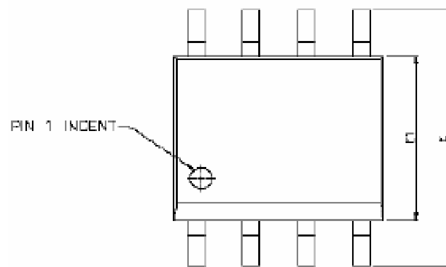
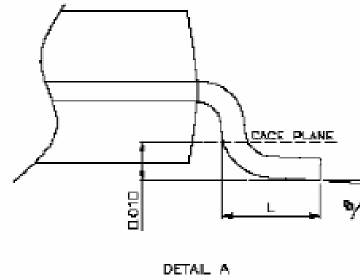
STP9527 Lead-free

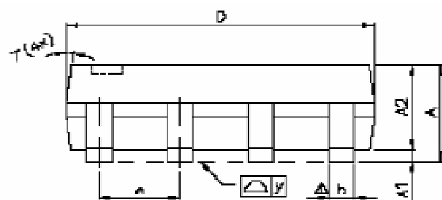
P Channel Enhancement Mode MOSFET

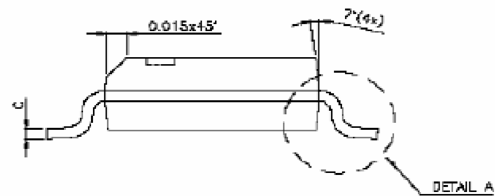
-10.0A

SOP-8 PACKAGE OUTLINE









SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	——	0.25	0.004	——	0.010
A2	——	1.45	——	——	0.057	——
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	——	1.27	——	——	0.050	——
L	0.38	0.71	1.27	0.015	0.028	0.050
⚠2 y	——	——	0.076	——	——	0.003
θ	0°	——	8°	0°	——	8°

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